10/044,427

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=> d his

     (FILE 'HOME' ENTERED AT 13:35:04 ON 17 SEP 2002)

     FILE 'REGISTRY' ENTERED AT 13:35:10 ON 17 SEP 2002
L1             11 S PHOSPHORUS ION?/CN

     FILE 'CAPLUS' ENTERED AT 13:37:27 ON 17 SEP 2002
L2           2325 S L1
L3          61373 S MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR VMO
L4            111 S L2 AND L3
L5              6 S L4 AND (PUNCHTHROUGH? OR PUNCH()THROUGH? OR WALK()OUT? OR WAL
L6           5203 S 400(2N)KEV OR FOUR()HUNDRED(2N)KEV OR 200(2N)KEV OR TWO()HUND
L7              1 S L6 AND L4
L8         891830 S SOURCE? OR CHANNEL?
L9             57 S L8 AND L4
L10             6 S L9 AND SHALLOW?
L11             5 S L10 NOT L5
L12        588147 S (ONE OR 1 OR TWO OR 2 OR THREE OR 3)(3N)(MICRON? OR MU OR MU(
L13            11 S L12 AND L4
L14            11 S L13 NOT L11
L15            10 S L14 NOT L5
L16            11 S RDSON OR ON()RESISTANCE?
L17             0 S L16 AND L4
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=> d l5 bib kwic 1-6

L5   ANSWER 1 OF 6  CAPLUS  COPYRIGHT 2002 ACS
AN   1999:281942  CAPLUS
DN   130:290242
TI   Fabrication of low mask count self-aligned silicided CMOS
     transistors with a high electrostatic discharge resistance
IN   Wu, Shye-lin
PA   Texas Instruments - Acer Incorporated, Taiwan
SO   U.S., 10 pp.
     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.       KIND  DATE          APPLICATION NO.  DATE
     ---------------  ----  --------      ---------------  --------
PI   US 5897348       A     19990427      US 1998-42351    19980313
RE.CNT  17    THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT
TI   Fabrication of low mask count self-aligned silicided CMOS
     transistors with a high electrostatic discharge resistance
AB   A method to fabricate simultaneously a CMOS transistor and an
     ESD protective transistor in a Si substrate is disclosed.  The
     NMOS transistor and PMOS transistor in the portion of
     the CMOS transistor have both anti-punch-
     through and salicide structures and individually with n-LDD and
     p-LDD structure, resp.  The structure of ESD protective devices is
     fabricated with self-aligned silicide but without LDD, thus the degrdn. of
     ESD protection can be solved.  The problems of accumulative aberration in
     scaled devices can also be alleviated through using blanket ion
     implantation technol. and salicide process to reduce the mask count as
     shown in the invention.
ST   fabrication CMOS silicided transistor electrostatic discharge
     protection
IT   Vapor deposition process
        (chem.; in fabrication of low mask count self-aligned silicided
        CMOS transistors with high electrostatic discharge resistance)
IT   MOS transistors
        (complementary; fabrication of low mask count self-aligned silicided
        CMOS transistors with high electrostatic discharge resistance)
IT   Electric discharge
     Semiconductor device fabrication
        (fabrication of low mask count self-aligned silicided CMOS
        transistors with high electrostatic discharge resistance)
IT   Transition metal silicides
     RL: DEV (Device component use); PNU (Preparation, unclassified); PREP
     (Preparation); USES (Uses)
        (fabrication of low mask count self-aligned silicided CMOS
        transistors with high electrostatic discharge resistance)
IT   Annealing
     Dielectric films
     Etching
     Ion implantation
     Siliconizing
        (in fabrication of low mask count self-aligned silicided CMOS
        transistors with high electrostatic discharge resistance)
IT   Coating materials
```

(masking; fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)
IT 7440-36-0, Antimony, uses 7440-38-2, Arsenic, uses 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
RL: MOA (Modifier or additive use); USES (Uses)
(dopant; in fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)
IT 11104-62-4P, Cobalt silicide 11129-80-9P, Platinum silicide 12627-41-7P, Tungsten silicide 12738-91-9P, Titanium silicide 39467-10-2P, Nickel silicide
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)
IT 12355-90-7, Boron difluoride(1+) 14594-80-0, Boron(1+), processes **16427-80-8**, Phosphorus(1+), processes 22679-96-5, Antimony(1+), processes 22856-08-2, Arsenic(1+), processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(implantation; in fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)
IT 7440-02-0, Nickel, processes 7440-06-4, Platinum, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-48-4, Cobalt, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of low mask count self-aligned silicided **CMOS** transistors with high electrostatic discharge resistance)

L5 ANSWER 2 OF 6 CAPLUS
AN 1997:362998 CAPLUS
DN 127:88760
TI Performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asymmetric/symmetric ion implantation
AU Ohzone, Takashi; Miyakawa, Tetsu; Matsuda, Toshihiro; Yabu, Toshiki; Odanaka, Shinji
CS Dep. Electronics Informatics, Toyama Prefectural Univ., Toyama, 939-03, Japan
SO IEEE International Conference on Microelectronic Test Structures Proceedings, Monterey, Calif., Mar. 17-20, 1997 (1997), 131-136 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 64KWAG
DT Conference
LA English
TI Performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asymmetric/symmetric ion implantation
AB 0.5 .mu.M **CMOS** ring-oscillators with LDD-type surface-channel n-**MOSFETs** and EPS-type buried-channel p-**MOSFETs** with asym./sym. source/drain fabricated by four kinds of ion-implantation methods were measured for evaluating the circuit performance. The ion-implantation methods were correlated to supply-current/oscillation-frequency/delay-power product and substrate current of the

ring-oscillator. The most preferable implantation method was the sym. 7.degree.x4-implantation in terms of circuit performance, asymmetry/mismatch and **punchthrough** immunity of **CMOSFET**
.

ST silicon **CMOS** ring oscillator ion implantation
IT **MOSFET** (transistors)
(complementary; performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asym./sym. ion implantation)
IT Integrated circuits
(ion implantation; performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asym./sym. ion implantation)
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asym./sym. ion implantation)
IT 12355-90-7, Boron difluoride 1+ **16427-80-8**, Phosphorus 1+, processes 22856-08-2, Arsenic 1+, processes
RL: DEV (Device component use); MOA (Modifier or additive use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(performance evaluation of **CMOS** ring-oscillators with source/drain regions fabricated by asym./sym. ion implantation)

L5 ANSWER 3 OF 6 CAPLUS COPYRIGHT 2002 ACS
AN 1989:488344 CAPLUS
DN 111:88344
TI Purification of phosphorus(2+) beam and anti-**punch-through** implantation of P-channel **MOSFET**
AU Li, Jinhua; Pan, Yiming
CS Shanghai Inst. Metall., Acad. Sin., Peop. Rep. China
SO Vacuum (1989), 39(2-4), 209-10
CODEN: VACUAV; ISSN: 0042-207X
DT Journal
LA English
TI Purification of phosphorus(2+) beam and anti-**punch-through** implantation of P-channel **MOSFET**
AB A purified P2+ beam was obtained by controlling the source pressure and the source magnet. It was used for anti-**punch-through** implantation of P-channel of **CMOS** devices with satisfactory results.
IT 14280-20-7, Boron(2+), properties 14594-80-0, Boron(1+), properties **16427-80-8**, Phosphorus(1+), properties
RL: PRP (Properties)
(implantation of silicon by)
IT **16427-81-9**, Phosphorus(2+), uses and miscellaneous
RL: USES (Uses)
(ion source for, for silicon transistor fabrication)

L5 ANSWER 4 OF 6 CAPLUS COPYRIGHT 2002 ACS
AN 1986:80101 CAPLUS
DN 104:80101
TI Design, modeling, and fabrication of subhalf-micrometer **CMOS** transistors
AU Schmitz, Adele E.; Chen, John Y.
CS Hughes Res. Lab., Malibu, CA, 90265, USA
SO IEEE Trans. Electron Devices (1986), ED-33(1), 148-53

CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
TI Design, modeling, and fabrication of subhalf-micrometer **CMOS** transistors
AB Two-dimensional process and device modeling was exercised extensively to det. the crit. process parameters for complementary **MOS** (**CMOS**) optimization. Buried-channel behavior of the p-channel FET's was analyzed. The effect of lightly doped drain (LDD) structure on **punch through** voltage was studied. p And n-channel FET's with phys. gate length as short as 0.3 .mu.m, were fabricated by using e-beam lithog., LDD structure, and silicided source-drains. The exptl. devices show high transconductance and long-channel characteristics.
ST complementary **MOS** transistor
IT Transistors
(complementary **MOS** subhalf-micron, design and modeling and fabrication of)
IT 14594-80-0, uses and miscellaneous **16427-80-8,** uses and miscellaneous 22856-08-2, uses and miscellaneous
RL: USES (Uses)
(implantation of, in subhalf-micron complementary **MOS** transistor fabrication)

L5 ANSWER 5 OF 6 CAPLUS COPYRIGHT 2002 ACS
AN 1985:124024 CAPLUS
DN 102:124024
TI **MOS field-effect transistor**
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 59165458	A2	19840918	JP 1983-39108	19830311

TI **MOS field-effect transistor**
AB Highly integratable **MOSFETs** with good **punch-through** potentials and high-speed performance are prepd. by forming a gate metal on a SiO_2 film on p-Si, implanting As^+ ions, covering with Si_3N_4, reactive-ion etching leaving the Si_3N_4 only on the contact sides, etching, implanting P^+ ions, annealing, coating with SiO_2, opening a window, depositing Al, and patterning.
ST **MOSFET** silicon silica aluminum
IT **16427-80-8,** uses and miscellaneous 22856-08-2, uses and miscellaneous
RL: USES (Uses)
(implantation doping of silicon by, in FET fabrication)

L5 ANSWER 6 OF 6 CAPLUS COPYRIGHT 2002 ACS
AN 1983:82070 CAPLUS
DN 98:82070
TI Threshold shift of p-channel transistors by boron implantation and the C-V characteristics of the corresponding **MOS** structures
AU Fang, R. C. Y.
CS Integr. Circuit Lab., Hewlet Packard Co., Palo Alto, CA, 94304, USA

SO Solid-State Electron. (1983), 26(1), 25-32
CODEN: SSELA5; ISSN: 0038-1101
DT Journal
LA English
TI Threshold shift of p-channel transistors by boron implantation and the C-V characteristics of the corresponding **MOS** structures
AB Short p-channel transistors for scaled complementary **MOS** circuits were fabricated using double implantations with P and B ions. Deep P channel implantation was required for increasing the channel **punch-through** voltage, while shallow B implantation was used to adjust the device threshold voltage for p-channel transistors with n + poly as the gate electrode. The effect of the B-dose and the subsurface junction depth on the device characteristics, esp. the capacitance-voltage (C-V) characteristics, was investigated. The capacitance dispersion with respect to frequency, which was obsd. for **MOS** diodes with a large B dose or deep B depth, is discussed. This phenomenon is explained by the majority carrier modulation at the subsurface junction assocd. with the B implanted channel. The effect of the nonuniform P channel doping on the measured C-V characteristics is examd. The technique of the 1-dimensional calcn. of the channel potential distribution is presented to show the correlation of the implanted B dose and the obsd. abnormal C-V characteristics.
ST silicon transistor boron implantation; capacitance voltage complementary **MOS**; phosphorus ion implantation transistor
IT Electric capacitance
(potential relations with, of **MOS** structures prepd. from boron-ion implanted p-channel transistors)
IT **16427-80-8**, properties
RL: PRP (Properties)
(implantation of p-channel transistors with, in **MOS** structure fabrication, capacitance-voltage characteristics in relation to)

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=> d l7 bib kwic 1

L7 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 1985:196002 CAPLUS
DN 102:196002
TI High energy ion implantation for C-**MOS** isolation n-wells technology: problems related to the use of multicharged phosphorous ions in an industrial context
AU Spinelli, P.; Escaron, J.; Soubie, A.; Bruel, M.
CS LETI, Commis. Energ. At., Grenoble, 38041, Fr.
SO Nucl. Instrum. Methods Phys. Res., Sect. B (1985), B6(1-2), 283-6
CODEN: NIMBEU
DT Journal
LA English
TI High energy ion implantation for C-**MOS** isolation n-wells technology: problems related to the use of multicharged phosphorous ions in an industrial context
AB High-energy ion implantation can be a very attractive technique for producing isolation wells in complementary **MOS** (**CMOS**) technol. This technique needs high-energy ion implantation equipment which is still rare and expensive, so the use of multicharged ions with a **200-keV** industrial machine could be a good alternate soln. Here, results obtained with the spreading-resistance technique on beveled samples of Si which have been implanted with triply charged P ions (600-**keV**), with a **200** DF-4 Extrion machine are presented. The high pressure in the extn. region leads to a mol. decompn. phenomenon and so induced errors into the true implanted dose and the in-depth P profile. These effects can be eliminated when PF5 is used as dopant gas in the source instead of PH3 + H2. However, the using of PF5 gives rise to a decrease in filament life. Some spreading-resistance profiles of high-energy P implantations are presented showing a strong channeling effect in the case of a normal incident ion beam.
ST ion implantation **MOS** isolation; complementary **MOS** isolation implantation; phosphorus ion implantation silicon
IT Semiconductor devices
(complementary **MOS**, high-energy ion implantation for prodn. of isolation wells in)
IT Ion beams
(high-energy implantation of, in prodn. of isolation wells in complementary **MOS** technol.)
IT **20337-88-6**, uses and miscellaneous
RL: USES (Uses)
(implantation of silicon with, in complementary **MOS** isolation n-well technol.)
IT 7440-21-3, uses and miscellaneous
RL: USES (Uses)
(implantation of, with triply charged phosphorus ions, in complementary **MOS** isolation n-well technol.)

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10/044,427

=> d l11 bib kwic 1-5

L11 ANSWER 1 OF 5 CAPLUS COPYRIGHT 2002 ACS
AN 2002:251893 CAPLUS
DN 136:271756
TI Formation of silicided ultra-**shallow** junctions using implant through metal technology and laser annealing process in fabrication of semiconductor devices
IN Chong, Yung Fu; Pey, Kin Leong; See, Alex
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6365446	B1	20020402	US 2000-609751	20000703
	US 2002098689	A1	20020725	US 2001-33284	20011231
PRAI	US 2000-609751	A3	20000703		

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT
TI Formation of silicided ultra-**shallow** junctions using implant through metal technology and laser annealing process in fabrication of semiconductor devices
AB A method is claimed for producing semiconductor devices such as **MOS** type transistors with deep **source**/drain junctions and thin, silicided contacts with desirable interfacial and elec. properties. The devices are produced by a method that involves pre-amorphization of the gate, **source** and drain regions by ion-implantation, the formation of a metal layer, ion implantation through the metal layer, the formation of a capping layer and a subsequent laser anneal.
IT Vapor deposition process
(chem.; formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT Etching
Gate contacts
Ion implantation
Laser annealing
Lithography
MOS transistors
Semiconductor device fabrication
Siliconizing
Sputtering
Vapor deposition process
p-n Semiconductor junctions
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT Metals, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)

IT Transition metal silicides
RL: SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT Amorphization
(ion-beam-induced; formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT 7440-02-0, Nickel, processes 7440-32-6, Titanium, processes 7440-48-4, Cobalt, processes 12623-53-9
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT 7440-21-3, Silicon, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT 7440-25-7, Tantalum, processes 7440-33-7, Tungsten, processes 12033-62-4, Tantalum nitride (TaN) 25583-20-4, Titanium nitride (TiN)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT 12355-90-7 14067-07-3, Silicon(1+), processes 14594-80-0, Boron(1+), processes 14791-69-6, Argon(1+), processes 15888-69-4, Germanium(1+), processes **16427-80-8**, Phosphorus(1+), processes 22856-08-2, Arsenic(1+), processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)
IT 7631-86-9, Silicon dioxide, processes 12033-89-5, Silicon nitride, processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(formation of silicided ultra-**shallow** junctions using implant through metal technol. and laser annealing process in fabrication of semiconductor devices)

L11 ANSWER 2 OF 5 CAPLUS COPYRIGHT 2002 ACS
AN 1999:538004 CAPLUS
DN 131:152685
TI Angled implant to build **MOS** transistors with narrow diffusion regions in contact holes
IN Kapoor, Ashok K.
PA National Semiconductor Corporation, USA
SO U.S., 18 pp.

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     CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.   DATE
     ---------------   ----  --------       ---------------   --------
PI   US 5943576         A    19990824       US 1998-145135    19980901
     US 6316318         B1   20011113       US 1999-333771    19990615
PRAI US 1998-145135     A1   19980901
RE.CNT  9      THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT
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TI Angled implant to build **MOS** transistors with narrow diffusion regions in contact holes

AB A method is described which forms an **MOS** transistor having a narrow diffusion region that is smaller than the diffusion region defined using photoresist in a conventional **CMOS** processing. In one embodiment, LOCOS can be used to form isolation (e.g., **shallow** trench) between active devices. A polysilicon layer is then deposited and doped either n+ or p+ selectively. The polysilicon layer is then patterned. Next, a dielec. layer and a refractory layer are deposited over the patterned polysilicon layer. Next, a contact hole with a high aspect ratio is defined in the oxide where the transistor will be formed. Angled implant of lightly-doped drain (LDD) regions or graft **source**/drain regions are formed on two opposite sides of the contact hole. The refractory metal layer is then removed. Spacers are then formed on opposite sidewall of the contact hole. A gate oxide layer is either thermally grown or deposited in the contact, before or after spacer formation. A gate material is then deposited into the contact hole to form a gate electrode. The gate electrode and the dielec. layer are polished to become coplanar.

ST implant doping fabrication **MOS** transistor contact hole

IT Dielectric films
Photolithography
Polishing
Polycrystalline films
(and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

IT Refractory metals
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

IT Contact holes
Doping
Gate contacts
Ion implantation
MOS transistors
(angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

IT Etching
(anisotropic; and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

IT Coating materials
(refractory; and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

IT Oxidation
(surface; and angled implant to build **MOS** transistors with

narrow diffusion regions in contact holes)
IT Oxidation
(thermal; and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)
IT 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(and angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)
IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)
IT 7440-33-7, Tungsten, uses 7440-38-2, Arsenic, uses 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
RL: MOA (Modifier or additive use); USES (Uses)
(angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)
IT 12355-90-7, Boron difluoride(1+) 14594-80-0, Boron(1+), processes **16427-80-8**, Phosphorus(1+), processes 22856-08-2, Arsenic(1+), processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(angled implant to build **MOS** transistors with narrow diffusion regions in contact holes)

L11 ANSWER 3 OF 5 CAPLUS COPYRIGHT 2002 ACS
AN 1999:426872 CAPLUS
DN 131:52783
TI Method to fabricate short-**channel MOSFETs** with an improvement in ESD resistance
IN Wu, Shye-lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5920774	A	19990706	US 1998-24772	19980217
	US 6187619	B1	20010213	US 1999-288948	19990409
PRAI	US 1998-24772	A2	19980217		

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT
TI Method to fabricate short-**channel MOSFETs** with an improvement in ESD resistance
AB A method to fabricate simultaneously a **MOS** transistor and an ESD protective transistor in a Si substrate is disclosed. The ESD protective devices are fabricated by using double diffused drain (DDD) ion implantation technol. In the functional region, **MOSFETs** structure are ion implanted by using a large angle pocket antipunchthrough, succeeded using a lightly doped drain implantation technol. with a liq. phase deposition (LPD) oxide layer in the ESD protective region as a mask. Next, a 1st thermal process is applied to form self-aligned silicide contacts. A low energy, high dose ion

implantation implanted into silicide is then carried out, which was used as a diffusion **source** for forming an ultra-**shallow** junction. After that, a 2nd rapid thermal process (RTP) is employed, an ultra-**shallow** junction, and low-resistivity stable phase of self-aligned silicide contacts in the functional region and a double diffusion junction in the ESD protective region are formed simultaneously.

ST **MOSFET** fabrication ESD resistance silicide

IT Vapor deposition process
(chem.; method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT Coating materials
(masking; method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT **MOS** transistors
MOSFET (transistors)
Semiconductor device fabrication
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance)

IT Doping
Electric contacts
Etching
Ion implantation
Photolithography
Rapid thermal annealing
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT Transition metal silicides
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT Electric discharge
(method to fabricate short-**channel MOSFETs** with improvement in ESD resistance)

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance)

IT 7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT 7440-02-0, Nickel, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent); USES (Uses)
(method to fabricate short-**channel MOS** transistors with improvement in ESD resistance using)

IT 11104-62-4P, Cobalt silicide 11105-01-4P, Silicon nitride oxide 12627-41-7P, Tungsten silicide 12738-91-9P, Titanium silicide 39467-10-2P, Nickel silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process);

USES (Uses)
(method to fabricate short-**channel** **MOS** transistors
with improvement in ESD resistance using)

IT 12355-90-7, Boron difluoride(1+) 14594-80-0, Boron(1+), processes
16427-80-8, Phosphorus(1+), processes 22679-96-5, Antimony(1+),
processes 22856-08-2, Arsenic(1+), processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical
process); PROC (Process); USES (Uses)
(method to fabricate short-**channel** **MOS** transistors
with improvement in ESD resistance using)

IT 10024-97-2, Nitrogen oxide (N2O), reactions 10102-43-9, Nitric oxide,
reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(method to fabricate short-**channel** **MOS** transistors
with improvement in ESD resistance using)

L11 ANSWER 4 OF 5 CAPLUS COPYRIGHT 2002 ACS
AN 1998:282368 CAPLUS
DN 128:329858
TI Method for manufacturing ISRC (inverted-sidewall recessed-**channel**
) **MOSFET**
IN Lee, Jong Duk; Chun, Kuk Jin; Park, Byung Gook; Lyu, Jeong Ho
PA Lee, Jong Duk, S. Korea; Korea Information & Communication Co., Ltd.
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5747356	A	19980505	US 1996-760490	19961205
	JP 09181316	A2	19970711	JP 1996-325250	19961205
PRAI	KR 1995-48511		19951206		

TI Method for manufacturing ISRC (inverted-sidewall recessed-**channel**
) **MOSFET**

AB The present invention provides a method for manufg. an ISRC (inverted-sidewall recessed-**channel**) **MOSFET**, comprising steps of forming an isolating layer through the LOCOS process, depositing a mask oxide layer, exposing only the part of silicon substrate for forming the **channel** and **shallow** junction of **source**/drain layers, depositing the first nitride layer over the resultant substrate, dry-etching the first nitride layer to form a nitride side-wall, forming an oxide layer being recessed into the **channel**, wet-etching the nitride side-wall, forming two doped layers for the **shallow** **source**/drain by an N+ or P+ ion-implantation, depositing the second nitride layer, dry-etching for forming a nitride side-wall, forming a P- or N- doped layer between the two doped layers, forming a gate oxide layer on the P- or N- doped layer, depositing a poly-silicon layer, forming a poly-silicon gate by a lithog. process and a dry-etching process, etching away the mask oxide layer, and ion-implanting for thick **source**/drain junction.

ST **MOSFET** inverted sidewall recessed **channel** manuf;
field effect transistor MOS ISRC
manuf

IT Doping
Ion implantation
MOSFET (transistors)

Semiconductor device fabrication
(method for manufg. ISRC (inverted-sidewall recessed-**channel**) **MOSFET**)

IT Nitrides
Oxides (inorganic), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for manufg. ISRC (inverted-sidewall recessed-**channel**) **MOSFET**)

IT 14158-23-7, Nitrogen(1+), uses **16050-72-9**, Phosphorus ion (P1-), uses **16427-80-8**, Phosphorus(1+), uses 17778-87-9, Nitrogen ion (N1-), uses
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(method for manufg. ISRC (inverted-sidewall recessed-**channel**) **MOSFET**)

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for manufg. ISRC (inverted-sidewall recessed-**channel**) **MOSFET**)

L11 ANSWER 5 OF 5 CAPLUS COPYRIGHT 2002 ACS

AN 1994:205875 CAPLUS

DN 120:205875

TI Elevated polycide **source**/drain **shallow** junctions with advanced silicidation processing and Al plug/collimated PVD (physical vapor deposition)-Ti/TiN/Ti/polycide contact for deep-submicron complementary metal-oxide semiconductors

AU Kotaki, Hiroshi; Takegawa, Yoshiyuki; Mori, Yukiko; Mitsuhashi, Katsumori; Takagi, Junkou

CS Cent. Res. Lab., Sharp Corp., Nara, 632, Japan

SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1994), 33(1B), 532-40
CODEN: JAPNDE; ISSN: 0021-4922

DT Journal

LA English

TI Elevated polycide **source**/drain **shallow** junctions with advanced silicidation processing and Al plug/collimated PVD (physical vapor deposition)-Ti/TiN/Ti/polycide contact for deep-submicron complementary metal-oxide semiconductors

AB Low-resistivity **shallow** junctions and completely filled contact technologies were developed. These were realized by forming the elevated polycide **source**/drain junction structure and Al plug/collimated PVD-Ti/TiN/Ti/Ti-polycide (APPOCIDE) contact structure through the use of advanced silicidation processes called AAS and BAS (As ions doped into the polycide layer after silicidation and B ions doped into the polycide layer after silicidation). About 2.0-2.1 .OMEGA./square sheet resistances of n+-Ti-polycide and p+-ti-polycide were reached at the same level as that of undoped Ti-polycide. Contact resistivities were (2-3) .times. 10-9 .OMEGA.-cm2 for a 0.35-.mu.m diam. contact on both n+ and p+. These contact resistivities were 2 orders of magnitude lower than that of the conventional Al/TiN/Ti/N+ or p+-Si structure. The authors proposed a unique consideration for the reasons for the relative difficulty in achieving silicidation with low sheet resistance of TiSi2 layer on n+-polysilicon as compared to that on undoped-polysilicon.

ST silicidation polycide **source** drain **shallow** junction

```
IT   Siliconization
        (of titanium in submicron CMOS device prepn.)
IT   Annealing
     Electric resistance
        (of titanium polycide in submicron CMOS device prepn.)
IT   Electric resistance
        (contact, of titanium polycide in submicron CMOS device
        prepn.)
IT   Semiconductor devices
        (microscale, complementary MOS, polycide fabrication of)
IT   Sputtering
        (radio-frequency, of titanium in submicron CMOS device
        prepn.)
IT   Nitridation
        (thermal, of titanium in submicron CMOS device prepn.)
IT   14594-80-0, Boron(1+), uses 16427-80-8, Phosphorus(1+), uses
     22856-08-2, Arsenic(1+), uses
     RL: USES (Uses)
        (implantation of, into polysilicon in polycide processing)
IT   12039-83-7, Titanium disilicide
     RL: DEV (Device component use); USES (Uses)
        (in polycide contacts for submicron CMOS devices)
IT   7631-86-9, Silica, uses
     RL: USES (Uses)
        (mask, for elevated polycide source/drain shallow
        junctions with advanced silicidation processing)
IT   7727-37-9
     RL: USES (Uses)
        (nitridation, thermal, of titanium in submicron CMOS device
        prepn.)
IT   72893-14-2, Aluminum 98, copper 0.5, silicon 1
     RL: DEV (Device component use); USES (Uses)
        (plug, for polycide contacts for submicron CMOS devices)
IT   7440-21-3, Silicon, uses
     RL: PRP (Properties)
        (polycryst., for elevated polycide source/drain
        shallow junctions with advanced silicidation processing)
IT   7440-21-3
     RL: USES (Uses)
        (siliconization, of titanium in submicron CMOS device prepn.)

=>
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=> d l15 bib kwic 1-7,9-10

L15 ANSWER 1 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1999:572469 CAPLUS
DN 131:315725
TI Evaluation of stabilization techniques for ion implant processing
AU Ross, Matthew F.; Wong, Selmer S.; Minter, Jason P.; Marlowe, Trey; Narcy, Mark E.; Livesay, William R.
CS Electron Vision Group, AlliedSignal Inc., San Diego, CA, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3678(Pt. 2, Advances in Resist Technology and Processing XVI), 1136-1156
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT
AB With the integration of high current ion implant processing into vol. **CMOS** manufg., the need for photoresist stabilization to achieve a stable ion implant process is crit. This study compares electron beam stabilization, a non-thermal process, with more traditional thermal stabilization techniques such as hot plate baking and vacuum oven processing. The electron beam processing is carried out in a flood exposure system with no active heating of the wafer. These stabilization techniques are applied to typical ion implant processes that might be found in a **CMOS** prodn. process flow. The stabilization processes are applied to a **1.1 .mu.**m thick PFI-38A i-line photoresist film prior to ion implant processing. Post stabilization CD variation is detailed with respect to wall slope and feature integrity. SEM photographs detail the effects of the stabilization technique on photoresist features. The thermal stability of the photoresist is shown for different levels of stabilization and post stabilization thermal cycling. Thermal flow stability of the photoresist is detailed via SEM photographs. A significant improvement in thermal stability is achieved with the electron beam process, such that photoresist features are stable to temps. in excess of 200.degree.. Ion implant processing parameters are evaluated and compared for the different stabilization methods. Ion implant system end-station chamber pressure is detailed as a function of ion implant process and stabilization condition. The ion implant process conditions are detailed for varying factors such as ion current, energy, and total dose. A redn. in the ion implant systems end-station chamber pressure is achieved with the electron beam stabilization process over the other techniques considered. This redn. in end-station chamber pressure is shown to provide a redn. in total process time for a given ion implant dose. Improvements in the ion implant process are detailed across several combinations of current and energy.
IT **16427-80-8**, Phosphorus(1+), uses
RL: NUU (Other use, unclassified); USES (Uses)
(evaluation of photoresist stabilization techniques for ion implant processing)

L15 ANSWER 2 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1997:563105 CAPLUS
DN 127:228078
TI Annealing behavior of a doubly MeV implanted silicon
AU Cho, Nam-Hoon; Huh, Tae-Hoon; Jang, Yoon-Taek; Ro, Jae-Sang; Oh, Jae-Geun;

Lee, Kil-Ho; Cho, Byung-Jin; Kim, Jong-Choul
CS Department of Metallurgy and Materials Science, Hong-Ik University, Seoul, 121-791, S. Korea
SO Ion Implantation Technology--96, Proceedings of the International Conference on Ion Implantation Technology, 11th, Austin, Tex., June 16-21, 1996 (1997), Meeting Date 1996, 661-664. Editor(s): Ishida, Emi. Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 64WFAP
DT Conference
LA English
AB MeV ion implantation has gained much attention in the field of **CMOS** retrograde well engineering. Damage formation by high-energy implantation has significant characteristics in that the lattice damage is concd. near Rp and isolated from the surface. Si self-interstitials are thought to be responsible for the formation of secondary defects upon annealing. The region of excess interstitials could be generated near Rp by two effects combined with Frenkel sepn. and dopant activation. However, at the same time, the small amt. of vacancy-rich zone may exist ahead of an interstitial-rich zone. In this study, the authors conducted model expts. to reveal the interactions between different types of defects upon annealing in a doubly MeV implanted silicon using ion species of P and C. The morphol. of secondary defects induced by P implantation in a doubly implanted sample was obsd. to be different from that in a singly P-implanted one. Meanwhile, no extended defects were obsd. in the C-implanted layer. DCXRD rocking curve analyses for the sample annealed at 550.degree. indicated that a pos. strain built up at .apprx.**2**
.3 .mu.m by P implantation was effectively reduced by .apprx.50% using addnl. carbon implantation. However, the amt. of strain relaxation in the C-implanted layer does not decrease upon annealing at 1000.degree..
IT 14067-05-1, Carbon(1+), uses **16427-80-8,** uses
RL: MOA (Modifier or additive use); USES (Uses)
(ion implant; annealing behavior of doubly MeV implanted silicon)

L15 ANSWER 3 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1989:488386 CAPLUS
DN 111:88386
TI Dual-type **CMOS** gate electrodes by dopant diffusion from silicide
AU Nygren, Stefan; Amm, David T.; Levy, Didier; Torres, Joaquin; Goltz, Gerhard; Ternisien D'Ouville, Thierry; Delpech, Philippe
CS Chem. Vieux-Chene, Cent. Natl. Etud. Telecommun., Meylan, F-38243, Fr.
SO IEEE Trans. Electron Devices (1989), 36(6), 1087-93
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
TI Dual-type **CMOS** gate electrodes by dopant diffusion from silicide
AB Dual work-function gate electrodes were implemented in a **1-.**
mu.m **CMOS** process. Dopant atoms were implanted into W silicide simultaneously with the source-drain implantations and subsequently diffused into the underlying polycryst. Si layer by rapid thermal annealing. As and B could easily be incorporated in the polysilicon to concns. >1020 cm-3. Capacitor and transistor measurements confirmed that n+ and p+-Si could be obtained, with a difference of .apprx.1 V between the resp. flat-band voltages. A very slight dose dependence was detected for As doses in the range from 1 .times. 1015 to 1 .times. 1016 cm-2, whereas a monotonous increase in the work function was

measured for increasing B doses in the same range. By comparison with conventional n-type gate **MOSFET**'s, it was verified that significantly improved subthreshold characteristics were obtained with p-type **PMOS** gate electrodes.

IT 14594-80-0, Boron(1+), uses and miscellaneous **16427-80-8**, Phosphorus(1+), uses and miscellaneous 22856-08-2, Arsenic(1+), uses and miscellaneous
RL: USES (Uses)
(gate electrodes from implantation of polysilicon and tungsten silicide by)

L15 ANSWER 4 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1989:16797 CAPLUS
DN 110:16797
TI Development of helium/chlorine based polysilicon etch process for use at a **1 micron** BICMOS gate/emitter poly etch
AU McOmber, Janice I.
CS Natl. Semicond., Santa Clara, CA, 95052-8090, USA
SO Proc. - Electrochem. Soc. (1988), 88-22(Proc. Symp. Plasma Process., 7th, 1988), 275-84
CODEN: PESODO; ISSN: 0161-6374
DT Journal
LA English
TI Development of helium/chlorine based polysilicon etch process for use at a **1 micron** BICMOS gate/emitter poly etch
AB A chlorine etch process is demonstrated which can be used to etch polysilicon to stop on single-crystal silicon for **1** to **2** **.mu.** bipolar and BICMOS applications. Proceduers used to minimize micromasking, Si roughness, and Si loss and control the polysilicon etch profile are discussed.
ST helium chlorine etching polysilicon; bipolar transistor polysilicon chlorine etching; **CMOS** transistor polysilicon chlorine etching
IT 14158-23-7, Nitrogen(1+), properties **16427-80-8**, Phosphorus(1+), properties
RL: PRP (Properties)
(helium-chlorine etching of polysilicon implanted with)

L15 ANSWER 5 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1986:120720 CAPLUS
DN 104:120720
TI Effects of various implant species and post-anneal treatments on silicon n-channel **MOSFETs**
AU Tseng, W. F.; Hevey, R. H.; Corazzi, R. J.; Christou, A.; Davis, G. E.
CS Nav. Res. Lab., Washington, DC, 20375-5000, USA
SO J. Electron. Mater. (1986), 15(1), 1-6
CODEN: JECMA5; ISSN: 0361-5235
DT Journal
LA English
TI Effects of various implant species and post-anneal treatments on silicon n-channel **MOSFETs**
AB A detailed anal. is presented of phys. and elec. characterizations of N-channel **MOSFETs** with gate lengths of **2-8** **.mu** .. The fabrication sequence features a self-aligned polysilicon gate and a LOCOS (local oxidn. of Si) process with variations in the source/drain implant species (As or P) and anneal ambients (dry O2 or N2). TEM micrographs show a difference in the defect configuration for As or P implants: As produces dislocation loops, while P produces a rigid

''square-grid'' dislocation network or an ''x'' or ''y'' shaped dislocation network depending on the anneal ambient. All defects terminate at the source/drain periphery for gate lengths .gtoreq.**2** **.mu.**. Elec. characterization shows typical **MOSFET** performance for devices with gate lengths >4 .mu.. The dry O2 anneal ambient apparently gives a slightly lower subthreshold leakage current (in the region of pA) than the N2 ambient. For devices with gate lengths of **2** **.mu.**, the depletion regions of the source and drain overlap and nearly overlap for the P and As cases, resp., due to fast diffusivity of P.

ST ion implantation silicon **MOSFET**

IT Electric current-potential relationship
(of silicon N-channel **MOSFETs**, effect of arsenic- and phosphorus-ion implantation on)

IT Transistors
(field-effect, N-channel **MOS**, effects of implant species and postanneal treatment on)

IT **16427-80-8**, properties 22856-08-2, properties
RL: PRP (Properties)
(current-voltage characteristics of silicon N-channel **MOSFETs** implanted with)

L15 ANSWER 6 OF 10 CAPLUS COPYRIGHT 2002 ACS

AN 1985:37675 CAPLUS

DN 102:37675

TI Realization of **1** **.mu.**m **CMOS** with tantalum disilicide (TaSi2) and separated self-aligned wells

AU Schwabe, Ulrich; Neppl, Franz; Jacobs, Erwin Peter; Takacs, Dezsoe

CS Forschungslab., Siemens A.-G., Munich, Fed. Rep. Ger.

SO Siemens Forsch.- Entwicklungsber. (1984), 13(5), 228-32
CODEN: SFEBBL; ISSN: 0370-9736

DT Journal

LA English

TI Realization of **1** **.mu.**m **CMOS** with tantalum disilicide (TaSi2) and separated self-aligned wells

AB A complementary **MOS** (**CMOS**) double-well technol. is presented which uses TaSi2 as gate and contact materials. The p-well is generated by 1.5 .times. 1012/cm2 B+ implantation at 160 keV and drive-in to **3**-6 **.mu.** depths into a 6-8 .mu.+ thick P+-doped n(100) 20 .OMEGA.-cm epilayer on an Sb-doped n(100) 0.02 .OMEGA.-cm substrate,. Self-aligned generation of the n-well is accomplished by local oxidn. of the p-well regions to 500 nm and by P implantation and drive-in to **1**-**1**.5 **.mu.**. Three-hundred nm cosputtered TaSi2 or 500 nm n+-poly-Si is used as gate material on 20-nm gate oxide. Results are presented for devices fabricated by using this process. While TaSi2 improves the performance of short-channel transistors, the proposed technol allows a significant redn. of the min. n+/p+ spacing without losing latchup hardness.

ST tantalum silicide complimentary **MOS** technol; **MOS** complementary sepd well technol; complementary **MOS** double well technol; transistor tantalum silicide gate

IT Semiconductor devices
Transistors
(**MOS**, with tantalum silicide gate and contact material and sepd. self-aligned wells)

IT 14594-80-0, uses and miscellaneous **16427-80-8**, uses and miscellaneous

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     RL: USES (Uses)
        (implantation of, self-aligned well formation by, in complementary
        MOS technol.)
IT   12039-79-1
     RL: USES (Uses)
        (in complementary MOS technol. with sepd. self-aligned wells)

L15  ANSWER 7 OF 10  CAPLUS  COPYRIGHT 2002 ACS
AN   1984:113390  CAPLUS
DN   100:113390
TI   Thin-film MOS field-effect
     transistor
PA   Hitachi, Ltd., Japan
SO   Jpn. Kokai Tokkyo Koho, 6 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1
     PATENT NO.       KIND  DATE          APPLICATION NO.  DATE
     ---------------  ----  --------      ---------------  --------
PI   JP 58192375       A2   19831109      JP 1982-75228    19820507
TI   Thin-film MOS field-effect
     transistor
AB   MOS transistors on optically transparent substrates with good
     elec. properties are fabricated by depositing a poly-Si film 1
     -10 .mu. on quartz at 200-1000.degree., depositing SiO2
     1 .mu., opening a window for sources and drains,
     implanting P+ ions and heating to form n+ sources and drains, field
     oxidizing the surface, removing the film sepg. the source and drain, and
     heating in a plasma contg. H2, F2, Cl2, Br2, or I2 at 200-1000.degree. to
     reduce the grain-boundary d.
ST   MOS transistor polysilicon; FET polysilicon silica; transistor
     polysilicon silica; phosphorus implantation silicon transistor; hydrogen
     halogen plasma silicon transistor
IT   Plasma, chemical and physical effects
        (halogen and hydrogen, for treatment of thin-film MOSFET)
IT   Halogens
     RL: USES (Uses)
        (plasma treatment of thin-film MOSFET by)
IT   16427-80-8, uses and miscellaneous
     RL: USES (Uses)
        (implantation by, of polysilicon for FET)
IT   7440-21-3, uses and miscellaneous
     RL: USES (Uses)
        (implantation of, with phosphorus ions during MOS device
        fabrication)
IT   7631-86-9, uses and miscellaneous
     RL: USES (Uses)
        (in thin-film MOSFET fabrication)
IT   1333-74-0, uses and miscellaneous
     RL: USES (Uses)
        (plasma treatment of polysilicon thin-film MOSFET by)

L15  ANSWER 9 OF 10  CAPLUS  COPYRIGHT 2002 ACS
AN   1982:627383  CAPLUS
DN   97:227383
TI   Improved dry etching resistance of electron-beam resist by ion exposure
```

process
AU Mochiji, Kozo; Wada, Yasuo; Obayashi, Hidehito
CS Cent. Res. Lab., Hitachi, Ltd., Tokyo, 185, Japan
SO J. Electrochem. Soc. (1982), 129(11), 2556-9
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB The dry etching resistance of a poly(Me methacrylate) electron-beam resist was successfully improved by P+ ion exposure prior to dry etching. The ion exposure increased resist stability by inhibiting deformation and reducing resist thickness loss during dry etching. It changed the chem. structure of the resist polymer into another material which was stable to dry etching. This technique was utilized for successful dry etching of **1 .mu.**m hole patterns in **MOS** LSI circuit manufg.
IT **16427-80-8**, uses and miscellaneous
RL: USES (Uses)
(bombardment by, of poly(Me methacrylate) electron-beam resist, for improved dry etching resistance)

L15 ANSWER 10 OF 10 CAPLUS COPYRIGHT 2002 ACS
AN 1976:188452 CAPLUS
DN 84:188452
TI The fabrication of an n-gallium arsenide thin layer by means of sulfur-ion implantation
AU Chang, Tung-Ho; Teng, Hsien-Tsan
CS Dep. Phys., Peking Norm. Univ., Peking, Peop. R. China
SO Inst. Phys. Conf. Ser. (1976), Volume Date 1975, 28(Appl. Ion Beams Mater.), 96-103
CODEN: IPHSAC
DT Journal
LA English
AB An n-type GaAs layer was produced in a Cr-doped semi-insulating GaAs substrate by implantation of 100 keV S+ ions at 1013 cm-2, with annealing at 825.degree. for 15 min. The implanted layer was .apprx.0.**2** -0.**3 .mu.**m thick, and had a mean carrier concn. of 5 .times. 1016-1017 cm-3, and a carrier mobility of 2600-3400 cm2/V-sec. The elec. properties of the layers were improved by an implantation with P+ after the S+. Schottky-barrier **field-effect transistors** employing implanted layers were comparable with those employing epitaxial layers with regard to transconductance and pinch-off voltage. Carrier concn. and mobility data are shown also for implantation with HS+ and H2S+.
IT **16427-80-8**, properties
RL: PRP (Properties)
(elec., of gallium arsenide layers implanted with sulfur and)

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?ds

Set     Items   Description
S1     185432   MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR -
             VMOS? OR DMOS? OR METAL()OXIDE()SEMICONDUCTOR?()FIELD()EFFECT-
             ()TRANSISTOR?
S2       6440   PHOSPHORUS(3N)ION? OR P(3N)ION?
S3       7125   (ION OR IMPLANT?) (3N) (PHOSPHORUS OR P)
S4       8745   S2 OR S3
S5       3643   S4 AND S1
S6       2987   PUNCHTHROUGH? OR PUNCH()THROUGH? OR WALKOUT? OR WALK()OUT?
S7        154   S6 AND S5
S8          9   S7 AND VERTICAL?
S9         56   400(2N)KEV OR FOUR()HUNDRED(2N)KEV OR 200(2N))KEV OR TWO()-
             HUNDRED(2N)KEV
S10         0   S9 AND S7
S11         2   S9 AND S5
S12      4111   RDSON OR ON()RESISTANCE?
S13         2   S12 AND S7
S14        40   S12 AND S5
S15        27   S14 AND ION?
S16   1453499   SOURCE? OR CHANNEL?
S17      1389   S16 (3N) SHALLOW?
S18        60   S17 AND S5
S19        55   S18 AND ION?
S20         2   S19 AND S6
S21         1   S19 AND S12
S22         0   S19 AND S9
S23    185468   (ONE OR 1 OR TWO OR 2 OR THREE OR 3) (3N) (MICRON? OR MU OR
              MU()MICRON? OR MICROMETER? OR MICROMETRE?)
S24       719   S23 (5N)S16
S25        13   S24 AND S5
?show files
File 344:Chinese Patents Abs Aug 1985-2002/Aug
         (c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/May(Updated 020903)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200259
         (c) 2002  Thomson Derwent
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
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?ds

Set      Items   Description
S1      185432   MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR -
                VMOS? OR DMOS? OR METAL()OXIDE()SEMICONDUCTOR?()FIELD()EFFECT-
                ()TRANSISTOR?
S2        6440   PHOSPHORUS(3N)ION? OR P(3N)ION?
S3        7125   (ION OR IMPLANT?) (3N) (PHOSPHORUS OR P)
S4        8745   S2 OR S3
S5        3643   S4 AND S1
S6        2987   PUNCHTHROUGH? OR PUNCH()THROUGH? OR WALKOUT? OR WALK()OUT?
S7         154   S6 AND S5
S8           9   S7 AND VERTICAL?
S9          56   400(2N)KEV OR FOUR()HUNDRED(2N)KEV OR 200(2N))KEV OR TWO()-
                HUNDRED(2N)KEV
S10          0   S9 AND S7
S11          2   S9 AND S5
S12       4111   RDSON OR ON()RESISTANCE?
S13          2   S12 AND S7
S14         40   S12 AND S5
S15         27   S14 AND ION?
?show files
File 344:Chinese Patents Abs Aug 1985-2002/Aug
         (c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/May(Updated 020903)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200259
         (c) 2002  Thomson Derwent
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
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?t s8/9/1-6

8/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05950403 **Image available**
SILICON CARBIDE **VERTICAL** **MOSFET** AND ITS MANUFACTURING METHOD

PUB. NO.: 10-233503 [JP 10233503 A]
PUBLISHED: September 02, 1998 (19980902)
INVENTOR(s): UENO KATSUNORI
APPLICANT(s): FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-036080 [JP 9736080]
FILED: February 20, 1997 (19970220)
INTL CLASS: [6] H01L-029/78; H01L-021/336
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R004 (PLASMA); R044 (CHEMISTRY -- Photosensitive Resins); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation

ABSTRACT

PROBLEM TO BE SOLVED: To provide higher withstand voltage of a **vertical** **MOSFET** using SiC.

SOLUTION: A selective ion **implantation** is performed with **phosphorus** **ion** using a wide mask, then a selective ion implantation is performed with boron ion using a narrower mask, and the mask is removed and thermal processing is performed to form a p-base region 33 and n-source region 34. Then a gate oxide film 35 is formed by thermal oxidation, and a gate electrode layer 36 of polycrystal silicon is formed. The length of a channel region 40 is designed independently of the thickness of the p-base region 33, respectively. For example, such structure of high dielectric strength as **punch** **through** is avoided in the channel region 40 can be provided. With the use of spacer, especially, the length of channel region 40 is formed with precision, for stable characteristics with good yield.

8/9/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04933908 **Image available**
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 07-226508 [JP 7226508 A]
PUBLISHED: August 22, 1995 (19950822)
INVENTOR(s): DEGUCHI TATSUYA
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-016888 [JP 9416888]
FILED: February 14, 1994 (19940214)
INTL CLASS: [6] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation

ABSTRACT

PURPOSE: To prevent the generation of a **punch** - **through** and a reduction in a carrier mobility in an FET and to contrive the speedup of a semiconductor device by a method wherein a gate and gate electrode are formed on a semiconductor substrate and impurity ions are implanted in the substrate obliquely to the substrate from two directions toward a gate length from both sides of the gate electrode.

CONSTITUTION: A field insulating film 2 is formed on a P-type silicon (a P-type Si) substrate 1 and a gate insulating film 3 consisting of a silicon

dioxide (SiO(sub 2)) film and a gate electrode 4 consisting of a polysilicon film are formed. Then, an N-type well 5 is formed by **implanting phosphorus ions** (**P** (sup +)) in the substrate 1 from both sides of the gate electrode 4 to the direction of a gate length in such a way as to tilt the ions at -40 deg. and +40 deg. to the **vertical** surfaces. An impurity profile in the wall 5 subsequent to the implantation becomes a composed one of a real line to show the oblique implantation from the right of a gate and dotted lines to show the oblique implantation from the left of the gate. A source 6 and a drain 6 are formed by implanting boron difluoride ions (BF(sup +2)). An interlayer insulating film 7 and wirings 8 are formed and the formation of the significant part of an FET ends.

8/9/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02633267 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 63-250167 [JP 63250167 A]
PUBLISHED: October 18, 1988 (19881018)
INVENTOR(s): FUKUI HIROKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-085964 [JP 8785964]
FILED: April 07, 1987 (19870407)
INTL CLASS: [4] H01L-027/06
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 715, Vol. 13, No. 62, Pg. 40, February 13, 1989 (19890213)

ABSTRACT

PURPOSE: To improve **punch - through** withstand voltage between a collector and an emitter without enlarging a film thickness of an epitaxial growth layer, by forming, through the same diffusion process, well regions of a C-**MOS** transistor element inside a base region directly under an emitter diffusion layer in a **vertical** type bipolar transistor.

CONSTITUTION: After P(sup +) burial layers 5a, 8, 9a, and N(sup +) burial layers 12 are formed on a P type semiconductor substrate 1, an N type epitaxial growth film 2 is made to grow. **Phosphorus ion implantation** processes are performed respectively in a region where a P-ch **MOS** transistor 20 is formed and in a region where a **vertical** type PNP transistor 40 is formed, and further N type well regions 4 and 11 are simultaneously formed. Because the formation of the N well region 11 then causes an impurity concentration of the N type epitaxial layer 2 in this region to be increased ten times or so, depletion layer's extension from a collector of the **vertical** type PNP transistor 40 to its emitter is perfectly stopped in this region, and so a **punch - through** withstand voltage can be set to 70V or more.

8/9/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02238665 **Image available**
INSULATED-GATE FIELD EFFECT TRANSISTOR AND MANUFACTURE THEREOF

PUB. NO.: 62-155565 [JP 62155565 A]
PUBLISHED: July 10, 1987 (19870710)
INVENTOR(s): MIZUNO TOMOHISA
SAWADA SHIZUO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 60-296001 [JP 85296001]
FILED: December 27, 1985 (19851227)
INTL CLASS: [4] H01L-029/78; H01L-021/265
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 567, Vol. 11, No. 390, Pg. 137, December 19, 1987 (19871219)

ABSTRACT

PURPOSE: To prevent deterioration of the reliability due to hot electrons by making the overlap lengths of the semiconductor layers for preventing **punch through** provided in the source and drain regions with the gate electrode be long for the source region side and short for the drain region side.

CONSTITUTION: A thermal oxide film 2 is formed on a substrate 1, phosphorus doped polycrystalline silicon 3 is deposited thereon, and patterning is performed, forming a gate electrode 3. Thereafter **phosphorus** is **ion - implanted** from a substantially **vertical** direction, and boron is ion-implanted at an incident angle with an inclination of, e.g., 45 deg., forming an N(sup -) layer 5 for LDD and a P(sup -) layer 4 for preventing **punch through** of a high impurity concentration from the substrate 1. Since the boron ions are implanted from a direction inclined toward the source region side, many boron ions are implanted into the source region side and a P(sup -) layer 4(sub s) of the source region side extends long under the gate electrode, and since the drain region side is in the shade of gate electrode, the ions are not implanted to much and the extension of a P(sup -) layer 4(sub d) of the drain region side becomes shorter than the N(sup -) layer.

8/9/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02134316 **Image available**
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 62-051216 [JP 62051216 A]
PUBLISHED: March 05, 1987 (19870305)
INVENTOR(s): MIZUNO TOMOHISA
SAWADA SHIZUO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-191569 [JP 85191569]
FILED: August 30, 1985 (19850830)
INTL CLASS: [4] H01L-021/265; H01L-029/60; H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 528, Vol. 11, No. 237, Pg. 151, August 04, 1987 (19870804)

ABSTRACT

PURPOSE: To prevent characteristic variation of transistors in a wafer plane and to enable making a wafer of a large diameter, by using the gate electrode as a mask, and by ion-implanting at least two times at the same implanting angle to the substrate plane to form desired diffusion layers.

CONSTITUTION: After a gate oxide film 12 is formed on the surface of a P-type silicon substrate 11, a phosphorus-doped polycrystalline silicon film is deposited and patterned to form a gate electrode 13. Next, using the gate electrode 13 as a mask, boron and **phosphorus** are sequentially **ion - implanted vertically** into the substrate 11, to form P(sup -) diffusion layers 14, 14 for preventing **punch - through** and N(sup -) diffusion layers 15, 15 constituting portions of source and drain regions. Next, using the gate electrode 13 and CVD oxide films 16, 16 formed on the side wall of the gate electrode 13 as a mask, **phosphorus** is **ion -**

implanted **vertically** into the substrate 11 to form N(sup +) diffusion layers 18, 18 constituting the source and drain regions. Since every diffusion layer formed in this way is symmetrical to the gate electrode, characteristic variation of transistors in the wafer plane can not occur.

8/9/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01520262 **Image available**
VERTICAL TYPE METAL OXIDE SEMICONDUCTOR TRANSISTOR

PUB. NO.: 59-231862 [JP 59231862 A]
PUBLISHED: December 26, 1984 (19841226)
INVENTOR(s): MIHARA TERUYOSHI
APPLICANT(s): NISSAN MOTOR CO LTD [000399] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-105544 [JP 83105544]
FILED: June 13, 1983 (19830613)
INTL CLASS: [3] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 313, Vol. 09, No. 106, Pg. 92, May 10, 1985 (19850510)

ABSTRACT

PURPOSE: To lower in resistance while avoiding the generation of a **punch - through** and a short channel effect by boring and forming a stopper groove into a first conduction type base body in parallel with the side surface of a second conduction type well region from the surface of the base body in addition to normal **vertical** type **MOS** transistor structure.

CONSTITUTION: An N(sup -) type layer 2 as a drain region is grown on an N(sup +) Si substrate 1 in an epitaxial manner, the whole surface is coated with a SiO(sub 2) film 20, and thickness on well and groove forming regions is thinned. The upper section of the groove forming region is coated with a resist film 21, B ions are implanted, ion implanted layers are formed in two well regions, and the P type well regions 3 are shaped through extension and diffusion. B ions are implanted to the surfaces of the central sections of the regions 3, **P ions** are **implanted** to both sides of the implantation regions while using resist films 23 as masks, and P(sup +) type well contact regions 9 and N(sup +) type source and drain regions 4 holding the regions 9 are shaped into the two regions 3 through extension and diffusion. Accordingly, a stopper region 11 is bored between the two regions 3.
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?t s11/9/1-2

11/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013718119 **Image available**
WPI Acc No: 2001-202343/200120
XRAM Acc No: C01-059998
XRPX Acc No: N01-144362
Robust latch-up immune MOSFET **structure manufacture, by forming p and n wells with barrier layers and n and p channel** MOSFET **'s respectively connected to reference potential and voltage supply respectively**
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHEN S; LEE J; SHIH J R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6190954	B1	20010220	US 99229381	A	19990111	200120	B

Priority Applications (No Type Date): US 99229381 A 19990111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6190954	B1		10	H01L-021/8238	

Abstract (Basic): US 6190954 B1
NOVELTY - Providing a robust latch-up immune **MOSFET** structure comprises:
(a) providing a p-type silicon substrate (11);
(b) forming a p-well (16) and an n-well (12) in the substrate;
(c) depositing a p-well barrier (42) and an n-well barrier (41), each of thickness 50-250 nm, in the p and n-well barriers respectively;
(d) creating p and n-channel **MOSFET** 's in the n and p-wells respectively;
(e) connecting the p-channel **MOSFET** to a voltage supply (15); and
(f) connecting the n-channel **MOSFET** to a reference potential (19).
USE - For forming a **CMOSFET** twin-well integrated circuit.
ADVANTAGE - The **MOSFET** structure is robust and latch-up immune, and the breakover voltage (VBO, trigger point) of the parasitic npn and pnp transistors is increased, due to the barrier layer which increases the energy gap for both electrons and holes.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through a twin well **CMOSFET** structure as formed above.
substrate (11)
n-well (12)
voltage supply (15)
p-well (16)
reference potential (19)
trench (31)
n-well barrier (41)
p-well barrier (42)
pp; 10 DwgNo 4a/9
Technology Focus:
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: The p-well barrier is doped with a group III element, e.g. B or BF2, by implanting to a concentration of 1013-15 atoms/cm2 at an energy of 50-200 KeV. The n-well barrier is doped with a group V element, e.g. **P** or As, by **implanting** to a concentration of 1013-15 atoms/cm2 at an energy of 250- **400 KeV** . The p-well barrier is between the bottom of the p-well and the n-channel **MOSFET** , and the n-well barrier is between the bottom of the n-well and the p-channel **MOSFET** . The p-well and the n-well are separated by a trench (31).
Title Terms: ROBUST; LATCH; UP; IMMUNE; **MOSFET** ; STRUCTURE; MANUFACTURE; FORMING; P; N; WELL; BARRIER; LAYER; N; P; CHANNEL; **MOSFET** ; RESPECTIVE; CONNECT; REFERENCE; POTENTIAL; VOLTAGE; SUPPLY; RESPECTIVE
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-021/8238
File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C02B; L04-E01B1
Manual Codes (EPI/S-X): U11-C02J6; U11-C18A3; U13-D02A; U13-E01

11/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013506729 **Image available**
WPI Acc No: 2000-678673/200066
XRAM Acc No: C00-206315
XRPX Acc No: N00-502371

Formation of an inductor on a silicon wafer substrate by reverse junctions

Patent Assignee: CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N); CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: SANDFORD CHU S; SHAO K; ZHU M; KAI S; MIN Z; SHAO-FU S C; CHU S S
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6133079	A	20001017	US 99358985	A	19990722	200066	B
EP 1071132	A2	20010124	EP 2000640001	A	20000310	200107	
SG 80666	A1	20010522	SG 996677	A	19991229	200134	
TW 434875	A	20010516	TW 99119087	A	19991102	200170	N

Priority Applications (No Type Date): US 99358985 A 19990722; TW 99119087 A 19991102
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133079	A		10	H01L-021/8238	
EP 1071132	A2	E		H01L-027/06	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SG 80666	A1			H01L-021/8238	
TW 434875	A			H01L-027/02	

Abstract (Basic): US 6133079 A

NOVELTY - An inductor is formed on a silicon wafer substrate (20) by reverse p/n junctions between a p-well and the p-type substrate.

DETAILED DESCRIPTION - Formation of an inductor on a silicon wafer substrate comprises providing a silicon wafer of a first conductivity type. A first photoresist layer (21) is patterned to define a first opening (23) in a region (22) of the wafer. A first dose of ions of a second conductivity type is implanted into the first opening at a first energy placing the centroid of the first dose at a first depth below the silicon surface, forming a pocket of the second conductivity type. The first photoresist layer is removed and the wafer is subjected to a first thermal annealing. A second photoresist layer defining a second opening is patterned wholly within and concentric with the first opening and spaced inward from the perimeter of the first opening by a gap. A second dose of ions of the first conductivity type is implanted at a second energy into the wafer, thus forming a well of the first conductivity type. The second dose is placed at a second depth which is shallower than t he first depth. The second photoresist layer is removed and the wafer is subjected to a second thermal annealing. Insulative layer(s) is formed over the region. An inductor element is formed on the insulative layers and lying entirely over the well. An INDEPENDENT CLAIM is also included for a method for forming a complementary metal-oxide semiconductor (**CMOS**) integrated circuit with an inductive element.

USE - For forming an inductor on a silicon wafer substrate.

ADVANTAGE - The method reduces inductor-to-substrate capacitance without requiring the application of electrical bias. It improves the high frequency performance of an inductor formed in an integrated circuit. It forms an inductor element in an integrated circuit with low substrate capacitance with low added process complexity.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of a region of a silicon wafer in which an inductor is formed.

Substrate (20)

Photoresist layer (21)
Region (22)
First opening (23)
pp; 10 DwgNo 3A/7

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Parameters: The first dose is 2x1012 - 3x1012 **ions** /cm2 of **phosphorus** and the first energy is **400** -450 **keV** . The first thermal annealing is conducted at 1000-1050degreesC and the first depth is 0.55-0.65 mum. The second dose is 1x1013 - 2x1013 ions/cm2 of boron and the second energy is 150-200 keV. The gap is 5-10 mum. Preferred Properties: The combined thickness of the insulative layer(s) is 2.5-5 mum. The planar dimensions of the first opening are 140x140 microns and that of the second opening are 125x125 microns The inductor lies within a planar region having dimensions of 100x100 microns.

Title Terms: FORMATION; INDUCTOR; SILICON; WAFER; SUBSTRATE; REVERSE; JUNCTION

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-021/8238; H01L-027/02; H01L-027/06

International Patent Class (Additional): H01L-021/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-B02C; L04-C02B; L04-C16

Manual Codes (EPI/S-X): U11-C08A1; U11-D03C3A; U12-C03; U12-Q; U13-D02A; U14-H03C2A

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15/9/1 **(Item 1 from file: 347)**
DIALOG(R)File 347:JAPIO

07056730 **Image available**
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 2001-284366 [JP 2001284366 A]
PUBLISHED: October 12, 2001 (20011012)
INVENTOR(s): IKUTA AKIHISA
NODA MASAAKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 2000-097957 [JP 200097957]
FILED: March 31, 2000 (20000331)
INTL CLASS: H01L-021/336; H01L-021/316; H01L-029/78

ABSTRACT

PROBLEM TO BE SOLVED: To realize a high withstand voltage and low **on - resistance** **DMOS** - structured device, having a tall and gentle step shape of an oxide film sandwiched between a conductive plate and a silicon substrate used in a high breakdown voltage semiconductor device.

SOLUTION: The semiconductor device manufacturing method comprises thermally oxidating a silicon substrate 1 to form a first silicon oxide film 10 on a silicon substrate 1, forming a second silicon oxide film 11 by chemical vapor deposition, forming **phosphorus ion implantion** regions 14 on the surface of the second silicon oxide film 11, forming a mask layer 3, and dipping in a solution containing hydrofluoric acid to etch the second and first silicon oxide films 11, 10 one after the other, thereby exposing the silicon substrate 1 surface. The slope angle of the oxide film steps can be controlled, by changing the dose of **phosphorus ions** in the **phosphorus ion implanting** regions 14.

15/9/2 **(Item 2 from file: 347)**
DIALOG(R)File 347:JAPIO

06427292 **Image available**
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-012855 [JP 2000012855 A]
PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): TAKAHASHI KENICHIRO
APPLICANT(s): NEC CORP
APPL. NO.: 10-179215 [JP 98179215]
FILED: June 25, 1998 (19980625)
INTL CLASS: H01L-029/78; H01L-021/8234; H01L-027/088

ABSTRACT

PROBLEM TO BE SOLVED: To make the occupied area reduction compatible with the breakdown voltage improvement by providing an extended drain layer on some of mutually contacted regions arranged from drains to sources, just beneath a selective oxide film.

SOLUTION: After forming high-breakdown voltage n-wells 16 at **PMOS** forming regions of a p-type semiconductor substrate 7 by **ion implantation** of **P** and hot intruding treatment, a thin oxide film 14 is formed by oxidation, a nitride film is deposited and grown thereon as an anti-oxidative film, a nitride film 15 on element-not-forming regions and extended drain regions 2 is etched to remove, a p-type stopper diffused layer 18 is formed **on resistances** at predetermined distances from p-type extended drain regions 19 and high-breakdown voltage n-wells 16 and oxidized to form a selective oxide film 12, after a photoresist 17 is removed, and an extended drain layer 19 is formed just beneath the selective oxide film 12.

15/9/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

05146996 **Image available**
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 08-102496 [JP 8102496 A]
PUBLISHED: April 16, 1996 (19960416)
INVENTOR(s): KIKUCHI SHUICHI
WATANABE YUICHI
MITSUSAKA EIICHI
TSUKADA YUJI
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-237479 [JP 94237479]
FILED: September 30, 1994 (19940930)
INTL CLASS: [6] H01L-021/8234; H01L-027/088; H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- **Ion** Implantation)

ABSTRACT

PURPOSE: To eliminate a gate offset region on the side of a source and reduce **on** - **resistance** of a transistor by a method wherein a thin film region of a gate oxide film forming a heavily doped source and drain layer is self-alizningly formed for a gate electrode of a high breakdown strength **MOS** transistor.

CONSTITUTION: A gate electrode 26B of a normal breakdown strength **MOS** transistor is formed on a thin gate oxide film 24 and a gate electrode 26A of a high breakdown strength **MOS** transistor is formed on a thick gate oxide film 22. With the use of these gate electrodes 26A, 26B as a mask, gate oxide films 24, 25 are dry-etched up to substantially 300 angstroms or less. Thereafter, (sup 31) **P** (sup +) **ions** are **ion** -implanted on one side of the gate electrode 26A, whereby a lightly doped drain layer 28 is formed. Next (sup 75)As(sup +) **ions** are **ion** -implanted, whereby heavily doped source and drain layers 30, 31 of a normal breakdown strength **MOS** transistor and heavily doped source and drain layers 32, 33 of a high breakdown strength **MOS** transistor are formed.

15/9/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03720856 **Image available**
SEMICONDUCTOR BIDIRECTIONAL SWITCH

PUB. NO.: 04-085956 [JP 4085956 A]
PUBLISHED: March 18, 1992 (19920318)
INVENTOR(s): MIHARA TERUYOSHI
APPLICANT(s): NISSAN MOTOR CO LTD [000399] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-199191 [JP 90199191]
FILED: July 30, 1990 (19900730)
INTL CLASS: [5] H01L-027/088; H01L-021/76; H01L-027/08
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 1229, Vol. 16, No. 307, Pg. 115, July 07, 1992 (19920707)

ABSTRACT

PURPOSE: To decrease **ON** **resistance** by surrounding transistors with channel cut regions and N(sup +) drift regions of the same conductivity type as a drift region and thereby separating a pair of **MOS** transistors

composing a semiconductor bidirectional switch from each other.

CONSTITUTION: An N/N(sup +) substrate is anisotropically etched to make grooves 11 at positions in where conductive channel cut regions 8 are to be formed. Conductive channel cut regions 8 are formed in the grooves 11 by deposition and etching back of amorphous silicon or polysilicon doped into N form and a gate oxide film 5 is formed. The polysilicon is deposited and patterned to form gate wirings 6 and boron **ions** are implanted with the gate wirings 6 used as masks to form channel regions 3. Source regions 4 are formed by selectively **implanting** **phosphorus** **ions** and arsenic **ions** . Layer insulating films 7 are deposited, contact holes 12 are made, and wirings 9 are formed. Thereby cell density is heightened and **ON resistance** is decreased through microstructure.
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?t s15/9/11,13,14,15,16,17,19,20

15/9/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

03484467 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 03-147367 [JP 3147367 A]
PUBLISHED: June 24, 1991 (19910624)
INVENTOR(s): SASE YASUKI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-285638 [JP 89285638]
FILED: November 01, 1989 (19891101)
INTL CLASS: [5] H01L-029/205; H01L-021/205; H01L-021/331; H01L-021/336; H01L-029/73; H01L-029/784
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 1113, Vol. 15, No. 371, Pg. 101, September 18, 1991 (19910918)

ABSTRACT
PURPOSE: To improve the **ON resistance** of a transistor by connecting a buried layer to the diffusion area from the surface in a drain part.

CONSTITUTION: A silicon oxide film 204 is made on a P-type silicon wafer 200, and the oxide film in the phosphorus buried region is removed 204 through a photoetching process. Then, a phosphorus buried layer 203 is made. And after removal of the oxide film 204, an epitaxial layer 206 of N-type silicon is formed. Then, after a silicon oxide film 207 is formed at the surface, the phosphorus diffused region is removed by etching, and the **ions** of **phosphorus** are **implanted** to form a **phosphorus** diffused region 205. Then, by annealing it, a phosphorus buried region 209 and the phosphorus diffused region 205 are connected. In this VDMOS transistor, drain current can be collected with an antimony buried layer 208 and taken out to the upper part through the phosphorus buried layer 209 and the phosphorus diffused layer 205.

15/9/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

02891575 **Image available**
DOUBLE-DIFFUSION TYPE FIELD EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 01-189175 [JP 1189175 A]
PUBLISHED: July 28, 1989 (19890728)
INVENTOR(s): SUZUMURA MASAHIKO
NOBE TAKESHI
AKIYAMA SHIGEO
APPLICANT(s): MATSUSHITA ELECTRIC WORKS LTD [000583] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-012829 [JP 8812829]
FILED: January 23, 1988 (19880123)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 838, Vol. 13, No. 481, Pg. 50, October 31, 1989 (19891031)

ABSTRACT
PURPOSE: To reduce loss and to enhance a heat resisting characteristic, by increasing impurity concentration in the surface of a conductivity type semiconductor region, where both diffused regions are not formed, in a

double-diffusion type FET, in which a gate electrode is formed on the surface region through an insulating layer.

CONSTITUTION: A mask 11 comprising an oxide film, which is provided on a semiconductor wafer 1, is used, and a P-type diffused region 2a is formed by impurity diffusion. Then, a mask 11' is used, and the region 2a is expanded sideward, and a P-type diffused region 2 is formed. Both diffused regions 2 and 3, which are self-aligned with the mask 11', are formed by double diffusions. Thereafter, the mask 11' is removed, and the regions 2 and 3 are once exposed. Then, a mask comprising a resist layer 12, which covers a part for a source electrode junction, is provided. Thereafter, **ions** of N-type impurities, e.g., **P** , are shallowly **implanted** in the surface as shown by dashed lines. Since the semiconductor has high withstand voltage and low **ON resistance** in this constitution, loss is little and a heat resisting characteristic is improved.

15/9/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

02674573 **Image available**
MANUFACTURE OF VERTICAL FIELD-EFFECT TRANSISTOR

PUB. NO.: 63-291473 [JP 63291473 A]
PUBLISHED: November 29, 1988 (19881129)
INVENTOR(s): YAMAMOTO MASANORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-126610 [JP 87126610]
FILED: May 22, 1987 (19870522)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- **Ion** Implantation)
JOURNAL: Section: E, Section No. 733, Vol. 13, No. 123, Pg. 47, March 27, 1989 (19890327)

ABSTRACT

PURPOSE: To reduce a P-type diffused region and to improve characteristics by decreasing an **ON resistance** by smoothly forming the shape of a depleted layer by utilizing an opening selectively formed in a silicon nitride film, and forming the P-type diffused region to improve its breakdown strength in one step.

CONSTITUTION: Silicon oxide films 6 are formed on the surfaces of an N(sup -) type epitaxial layer 2 exposed in an opening 5 and a polycrystalline silicon layer 4. Then, silicon nitride films 7 are deposited on the films 6, and selectively etched to form an opening 8 smaller than the opening 5 at the center of the opening 5. Then, with the layer 4 as a mask impurity **ions** are **implanted** to form **P** (sup +) type diffused regions 9 deeply in the opening 8 having only the film 6 on an N(sup -) type epitaxial layer 2 and shallowly in the opening 5 laminated with the films 7, 6 except the opening 8. Thus, the diffused region per unit cell can be reduced, the **ON resistance** of a vertical field-effect transistor is effectively reduced, and the characteristics can be improved.

15/9/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

02645973 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 63-262873 [JP 63262873 A]
PUBLISHED: October 31, 1988 (19881031)
INVENTOR(s): YOU SEIHATSU
TANIDA YUJI

APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-098109 [JP 8798109]
FILED: April 21, 1987 (19870421)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 719, Vol. 13, No. 81, Pg. 164, February 23, 1989 (19890223)

ABSTRACT
PURPOSE: To lower **ON resistance** largely, to enable large conduction without damaging breakdown strength and to reduce an occupying area by removing an offset region on the source side of a high breakdown-strength insulated gate **MOSFET** .

CONSTITUTION: **P ions** are **implanted** into regions 7-1, 7-2 surrounding a drain in a P-type Si substrate 1 and an offset region 70 to form the N(sup -) layers 7-1, 7-2, 70. The N(sup -) layers are coated with LOCOS insulating films 6-1-6-3 and a gate oxide film 4. A poly Si gate electrode 5 to which P is added in high concentration is shaped to coat the LOCOS insulating films 6-1-6-3, adjacent gates 5 are connected mutually, and the partial offset 70 being in contact with a source 2 is positioned under a gate electrode 50. **P ions** are **implanted** to form N(sup +) drains 3-1, 3-2 and a source 2-2. Inter-layer insulation is conducted by a BPSG film 8, and a source electrode and a drain electrode 11 in Al are shaped and coated with a protective film, thus completing a semiconductor device. According to the constitution, **ON resistance** can be lowered without damaging breakdown strength, and a channel is also formed to the layer 70 by shaping the offset layer 70 connected to an adjacent drain at the time of the parallelism of a FET, thus causing large currents to flow.

15/9/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

02538867 **Image available**
INSULATED GATE TYPE FIELD EFFECT TRANSISTOR

PUB. NO.: 63-155767 [JP 63155767 A]
PUBLISHED: June 28, 1988 (19880628)
INVENTOR(s): MORIKAWA MASATOSHI
YOSHIDA ISAO
OTAKA SHIGEO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-301235 [JP 86301235]
FILED: December 19, 1986 (19861219)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 678, Vol. 12, No. 418, Pg. 85, November 07, 1988 (19881107)

ABSTRACT
PURPOSE: To reduce a dimension and to decrease an **on - resistance** , by forming a part of a source region upwardly on a surface of a substrate.

CONSTITUTION: A gate oxidizing film 7 is formed in a recessed shape on a substrate, and a base region 3 is formed and thereafter undoped polycrystal silicon is piled all over the surface in order to form a gate electrode 6 and an external source region 8. Then, after the surface is flattened, it is irradiated with **phosphorus ion** beams 12. **Phosphorus** in polycrystal silicon is diffused into the base region, and next a source region 4 is formed, and thereafter phosphorus glass 10 is piled all over the surface. After heat treatment is performed for this substrate, etching is performed

for formation of a base drawing region 5. Then, with the region 5 used as a mask, boron **ion** beams are radiated. Successively, the surface of the region 5 and the side of the region 8 are cleaned by a dry etching method, and next aluminium is stuck thereon so as to form a source drawing electrode 9.

15/9/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

02404975 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 63-021875 [JP 63021875 A]
PUBLISHED: January 29, 1988 (19880129)
INVENTOR(s): HASHIZUME SHINGO
UMEBACHI SHOTARO
APPLICANT(s): MATSUSHITA ELECTRONICS CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-166969 [JP 86166969]
FILED: July 16, 1986 (19860716)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- **Ion** Implantation)
JOURNAL: Section: E, Section No. 627, Vol. 12, No. 228, Pg. 163, June 28, 1988 (19880628)

ABSTRACT

PURPOSE: To reduce an **ON resistance** at the time of operating a vertical **MOSFET** thereby to improve the high speed operability of a semiconductor device by forming the same conductivity type high density region as a substrate on the surface of the substrate.

CONSTITUTION: A preparing region of a P-type impurity region 6 and a gate oxide film 4 are formed on an N-type substrate 5, with a resist 9 as a mask **phosphorus ions** are **implanted** to form the preparing region of an N-type high impurity region 8. Then, a polycrystalline silicon 2 is deposited, a gate electrode pattern is formed by plasma etching, boron **ions** are implanted, and thermally diffused to form a P-type channel region 7. Thereafter, with the resist pattern 9 and the silicon 2 as masks **phosphorus ions** are **implanted** to form an N-type source region 3, a protecting film 10 is deposited, a window is selectively opened thereat, and a source electrode 1 is formed. Thus, an **ON resistance** can be reduced.

15/9/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO

02101867 **Image available**
VERTICAL TYPE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 62-018767 [JP 62018767 A]
PUBLISHED: January 27, 1987 (19870127)
INVENTOR(s): SASAKI YOSHITAKA
APPLICANT(s): TDK CORP [000306] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-157819 [JP 85157819]
FILED: July 17, 1985 (19850717)
INTL CLASS: [4] H01L-029/78; H01L-029/52
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 517, Vol. 11, No. 190, Pg. 40, June 18, 1987 (19870618)

ABSTRACT
PURPOSE: To obtain a vertical FET having fast switching velocity by superposing a polysilicon and a resist mask on an oxide film of an N-type Si layer, etching to form overhangs, reactively **ion** -etched to form a groove, forming a shallow P-type layer and mainly an N(sup +) type source around the wall of the groove by utilizing a deep P(sup +) type layer and a polysilicon gate in the groove.

CONSTITUTION: A non-doped polysilicon 6a is superposed on a gate oxide film 5a on an N-type layer 2 on an N(sup +) type Si substrate 1, a resist mask 7 is applied, etched to form overhangs, reactively **ion** -etched to form a vertical groove 3b. **Ions** 3a are implanted, heat treated to form a P(sup +) type layer 3, then with a layer 6a as a mask a shallow P-type layer 4 partly superposed under the end of the film 6a by **ion** implanting and heat treating, V(sub th) is decided by the **ion** implanting amount, and a channel width is decided in the diffusing length of the **P** -type layer. Then, **ions** 8a are implanted, an SiO(sub 2) 5b, a PSG 5c are superposed and heat-treated to diffuse an N(sup +) type layer 9, and an electrode 11 is attached. According to this configuration, since a P-channel region 4 is narrow, a large power vertical FET having large g(sub m), a fast switching velocity and low **ON resistance** is obtained.

15/9/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO

02101866 **Image available**
MANUFACTURE OF VERTICAL TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 62-018766 [JP 62018766 A]
PUBLISHED: January 27, 1987 (19870127)
INVENTOR(s): SASAKI YOSHITAKA
APPLICANT(s): TDK CORP [000306] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-157818 [JP 85157818]
FILED: July 17, 1985 (19850717)
INTL CLASS: [4] H01L-029/78; H01L-029/52
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- **Ion** Implantation)
JOURNAL: Section: E, Section No. 517, Vol. 11, No. 190, Pg. 40, June 18, 1987 (19870618)

ABSTRACT
PURPOSE: To enhance the switching velocity by forming a **P** -channel by **ion implantation** through the exposed end of a polysilicon gate film and a gate oxide film, uniforming the density of an N-type Si substrate, and reducing the channel length as small as possible irrespective of the formation of an N(sup +) type source layer.

CONSTITUTION: A gate oxide film 5a, a polysilicon 6a and a PSG 5b are superposed on an N-type layer 2 on an N(sup +) type Si substrate 1, a resist mask 7a is applied, etched to form overhangs as a **P** -type **ion** - **implanted** region 3a. The only PSG 5b is selectively etched, and removed to expose the film end 6a(sub 1). The mask 7a is removed, B **ions** are implanted at 4a by the mask 5b, heat- treated to form a P-channel 4b. Then, the resist mask 7b is applied, **P ions** 8a are **implanted** , the mask 7b is removed, a PSG 5d is spread, heat-treated to form an N(sup +) type source 8, an electrode 9 is attached to complete this device. According to this configuration, the length of the channel 4b can be extremely shortened and g(sub m) can be increased. Accordingly, an **ON resistance** decreases to improve the switching velocity, and since the density in the channel is uniform, V(sub th) is not irregular.
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?t s15/9/22,24,25,27

15/9/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

02094375 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 62-011275 [JP 62011275 A]
PUBLISHED: January 20, 1987 (19870120)
INVENTOR(s): YOSHIDA ISAO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-167924 [JP 86167924]
FILED: July 18, 1986 (19860718)
INTL CLASS: [4] H01L-029/78; H01L-029/52
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 514, Vol. 11, No. 179, Pg. 56, June 09, 1987 (19870609)

ABSTRACT

PURPOSE: To obtain a vertical IGFET with a low **ON** **resistance** and a high output power by providing a high concentration impurity layer in the surface part of a common drain layer.

CONSTITUTION: An SiO(sub 2) film 17 on a P-type Si substrate 1 is selectively removed and **P** **ions** are **implanted** 12 to form an N-type layer 2. An aperture is drilled in an SiO(sub 2) film 17' produced in an annealing process to form an N(sup +) type substrate contact layer 13. If a gate oxide film 6 is formed by removing the SiO(sub 2) film selectively, the remaining part 19 has a large film thickness. Polycrystalline Si 5' is applied to form a gate electrode 5 and **ions** are implanted 14 to form an N(sup -) type layer 3 between the adjacent electrodes 5 and form an N(sup -) type layer 4' around the N(sup +) type layer 13. Then the surface is covered with SiO(sub 2) 16 and an aperture is drilled to form an N-type source 4 by diffusion. Then the surface is covered with PSG 10 and an aperture is drilled to provide an Al source electrode and gate lead-out electrode, which is not shown, and an Au film 8 is applied to the back plane to complete the device. With this constitution, an **ON** **resistance** can be reduce significantly.

15/9/24 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

00891864 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 57-042164 [JP 57042164 A]
PUBLISHED: March 09, 1982 (19820309)
INVENTOR(s): ITO HIDESHI
ITO MITSUO
OTAKA SHIGEO
ASHIKAWA KAZUTOSHI
IIJIMA TETSUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-117093 [JP 80117093]
FILED: August 27, 1980 (19800827)
INTL CLASS: [3] H01L-029/78; H01L-029/06; H01L-029/36
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- **Ion** Implantation)
JOURNAL: Section: E, Section No. 114, Vol. 06, No. 111, Pg. 146, June 22, 1982 (19820622)

ABSTRACT

PURPOSE: To avoid the lowering of a withstand voltage while reducing the **ON resistance** by making the concentration of the impurity on the bottom of an epitaxial layer higher than that on the top and the surrounding part of the layer to become a drain region composing a vertical type **MOSFET** .

CONSTITUTION: An n(sup -) type layer 8 with a concentration of about 10(sup 15)/cm(sup 2) is epitaxially grown on an n(sup +) type Si substrate 10 with an impurity concentration of about 10(sup 21)/cm(sup 2) and after the surface thereof is covered with an oxide film 11, an n type impurity **ion** is implanted into the layer 8 therethrough to be turned to a 3- layer construction comprising an n(sup +) type layer 8A at the top, an n type 8B at the medium and an n(sup -) type layer (the layer 8 left as intact) at the bottom. Then, a **p** type impurity **ion** is shallowly implanted at a low concentration into a region 9 to be a channel section while a p(sup +) type region 12 is formed for a contact section likewise by **ion** implantation in such a manner as to stay within the layer 8C passing through the channel region 9. Thereafter, a thin n(sup +) type source region 13 is formed across the regions 9 and 12 by diffusion. In this manner, only the bottom of the layer 8 to be the drain region is high in the concentration to reduce the **ON resistance** while the bottom of the channel section comes in contact with the layer 8 low in the concentration thereby avoiding the lowering of the withstand voltage.

15/9/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

00464885
FIELD EFFECT TRANSISTOR OF INSULATION GATE TYPE AND ITS MANUFACTURE

PUB. NO.: 54-116885 [JP 54116885 A]
PUBLISHED: September 11, 1979 (19790911)
INVENTOR(s): YOSHIDA ISAO
YAMAGUCHI KEN
OKABE TAKEAKI
MASUHARA TOSHIAKI
SAKAI YOSHIO
KOYANAGI MITSUMASA
OCHI SHIKAYUKI
ITO HIDESHI
NAGATA MINORU
HASHIMOTO TETSUKAZU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 53-023485 [JP 7823485]
FILED: March 03, 1978 (19780303)
INTL CLASS: [2] H01L-029/78; H01L-029/06; H01L-029/60
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 152, Vol. 03, No. 139, Pg. 66, November 17, 1979 (19791117)

ABSTRACT

PURPOSE: To increase a high current without a decrease in dielectric strength by making the gate film of a depletion region thicker than any other one by providing a resistance region to an offset part and by making uneven the threshold voltage of a channel under a gate electrode.

CONSTITUTION: To P-type Sil, N-type source and drain 2 and 3 are provided and then covered with gate oxidized film 9. Film 10 is a separating oxidized film. Next, layer 13 is formed by **implanting phosphorus ions** . Layer 13 is etched partially to form enhancement channel 12, which is covered with thermal oxidized film 82, so that high resistance layer 4 will be produced. Next, an electrode window is etched selectively and electrodes 5 to 7 are provided. By this method, the enhancement channel length depends upon the mask length for selective etching; the manufacture is simple, **ON**

resistance is low, and mutual conductance is high, so that a high-output **MOSFET** can be obtained.

15/9/27 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008306116 **Image available**
WPI Acc No: 1990-193117/199025
Related WPI Acc No: 1989-309000
XRPX Acc No: N90-150256

Voltage threshold setting method for power MOSFET **- uses substrate having three layers of differing conductivity and anisotropically etched groove**

Patent Assignee: GEN INSTR CORP (GENN)
Inventor: EINTHOVEN W G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4929987	A	19900529	US 89358883	A	19890530	199025	B

Priority Applications (No Type Date): US 89358883 A 19890530; US 88150755 A 19880201

Abstract (Basic): US 4929987 A

The wafer with a 100 orientation comprises N layer (middle layer) and a lightly doped P layer (top layer). A strongly doped N layer (source layer) is diffused into most of the top layer. An oxide layer is grown. A V groove with a flat bottom is anisotropically etched through openings in the oxide layer. The V groove is etched through the source layer and most of the P layer. The bottom of the groove initially is at a level above the junction between the top layer and the middle layer. Exposure to beam of **phosphorus ions** forms a shallow implanted channel region proximate the walls of the groove. An unwanted implanted region along the bottom of the groove is also formed.

A second anisotropic etch, through the same oxide mask, deepens the groove bottom to a point below the junction, removing the unwanted portion of the implanted region along the groove bottom. The implanted concentration of the channel is later reduced as the gate oxide is formed. This method of groove formation can be used to set the threshold voltage of enhancement mode power **MOSFETS** .

ADVANTAGE - Provides method for setting threshold voltage without compromising other parameters. Can also be used to produce depletion mode power **MOSFETS** with zero-gate **on resistance** values of a few MILLI-OHM CM(2).

Dwg.4/4

Title Terms: VOLTAGE; THRESHOLD; SET; METHOD; POWER; **MOSFET** ; SUBSTRATE; THREE; LAYER; DIFFER; CONDUCTING; ANISOTROPE; ETCH; GROOVE
Derwent Class: U12
International Patent Class (Additional): H01L-029/78
File Segment: EPI
Manual Codes (EPI/S-X): U12-D02A; U12-E01
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?t s20/9/1-2

20/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01096470 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 58-033870 [JP 58033870 A]
PUBLISHED: February 28, 1983 (19830228)
INVENTOR(s): SUNAMI HIDEO
MASUDA HIROO
KAMIGAKI YOSHIAKI
SHIMOHIGASHI KATSUHIRO
TAKEDA EIJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-131521 [JP 81131521]
FILED: August 24, 1981 (19810824)
INTL CLASS: [3] H01L-029/78; H01L-029/36
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**)
JOURNAL: Section: E, Section No. 176, Vol. 07, No. 115, Pg. 9, May 19, 1983 (19830519)

ABSTRACT

PURPOSE: To improve the mobility of carrier and to enable the control of a threshold voltage of a semiconductor device by superposing the structures of **punch through** stopper type and low oblique type and further introducing an impurity of reverse conductive type to the substrate to the vicinity of the Si surface.

CONSTITUTION: A gate oxidized film 2 is formed on a p type Si substrate 1. Thereafter, B **ions** are **implanted** , thereby forming a **p** type layer 8. Impurity **ions** becoming n type layer 8 of the reverse conductive type to the substrate are implanted. Thereafter, a gate 3 is covered, and As **ions** are implanted in the overall surface. Thus, an n(sup +) type layer which has low withstand voltage between the **source** and the drain, **shallow** junction and low resistance is formed. In order to control the decrease in the withstand voltage, **P** **ions** are **implanted** , thereby forming a **P** type diffused layer 7. Subsequently, an insulating film 4 is covered, an electrode 5 connected to the source and drain 6 is covered on the film, thereby forming an **MOS** transistor.

20/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013814523 **Image available**
WPI Acc No: 2001-298735/200131
Related WPI Acc No: 1999-394745
XRAM Acc No: C01-091818
XRPX Acc No: N01-214102

Fabrication of metal oxide semiconductor transistor (MOST) and electrostatic discharge protective transistor in silicon substrate includes forming a silicide layer, ultra-shallow junctions and double diffused drain junctions

Patent Assignee: WU S (WUSS-I)
Inventor: WU S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6187619	B1	20010213	US 9824772	A	19980217	200131	B
			US 99288948	A	19990409		

Priority Applications (No Type Date): US 99288948 A 19990409; US 9824772 A 19980217

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6187619	B1		10	H01L-021/8238	CIP of application US 9824772
					CIP of patent US 5920774

Abstract (Basic): US 6187619 B1

NOVELTY - A metal oxide semiconductor (**MOS**) transistor and an electrostatic discharge (ESD) protective transistor are fabricated in a silicon substrate by forming in a functional region (20) a lightly doped drain (LDD) region, an anti- **punch** **through** region, a silicide layer and ultra-shallow junctions. In an ESD protective region (21), an LDD region and double diffused drain (DDD) junctions are formed.

DETAILED DESCRIPTION - Fabrication of a **MOS** transistor and an ESD protective transistor in a silicon substrate comprises providing an isolation region (24) in the substrate to separate a functional region which has a first poly-gate (22) from an ESD protective region which has a second poly-gate and a first insulating layer (25) is formed on all resulting surfaces. A first **ion** implantation is performed to all resulting surfaces using first conductive **ions** to form a first and a second LDD region in the functional region and in the ESD protective region, respectively. A second **ion** implantation is performed with a tilted angle to all resulting surfaces using second conductive **ions** having an opposite electrical conductivity to the first conductive **ions** to form a first anti- **punch** **through** region (30) beneath the second poly-gate. After the functional region is masked by using a photoresist layer, a third **ion** implantation is performed with a tilted angle to the ESD protective region using two kinds of the first conductive **ions** co-implanted to form a doped region (32) beneath the second poly-gate. A second insulating layer is formed on the ESD protective region using the photoresist layer as a mask, then the photoresist layer is removed. Dielectric spacers (36) are formed on sidewalls of the first poly-gate and on a portion of the first LDD region using the second insulating layer as the mask so that a remnant of the LDD regions serves as first source/drain (S/D) region. A self-aligned silicide layer (38) is formed on the first poly-gate and on the first S/D region. A fourth **ion** implantation is performed to all resulting surfaces to form the first S/D region in the functional region using the second insulating layer as the mask. A third insulating layer is formed on all resulting surfaces and a thermal annealing is performed to the substrate to form ultra-shallow junctions and DDD junctions in the functional region and in the ESD protective region, respectively.

USE - Fabricating a **MOS** transistor and an ESD protective transistor in a silicon substrate.

ADVANTAGE - By using silicide layer as a diffusion **source** , ultra- **shallow** junctions with self-aligned silicide contacts in the functional devices could be obtained. The circuit operation speed and the short channel effect in the functional devices could be improved. By using the DDD junction, high protection voltage could be obtained.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a self-aligned silicide on S/D region, poly-gate of the functional region during formation.

Functional region (20)
ESD protective region (21)
Poly-gates (22)
Isolation regions (24)
Insulating layers (25)
Anti- **punch** **through** regions (30)
Doped regions (32)
LPD oxide (33)
Dielectric spacers (36)
Silicide layers (38)
pp; 10 DwgNo 8/10

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Components: The first insulating layer is an oxynitride layer, while the third insulating layer is an oxide layer which is 100-800 nm thick. The dielectric spacers are oxide or nitride spacers, and the metal layer is titanium, cobalt, nickel or tungsten. Preferred **Ions** : The first

conductive **ions** are arsenic (Ar), **phosphorus** (P) or antimony (Sb) for forming an **NMOS** transistor; or boron (B) or difluoroborate (BF2) for forming a **PMOS** transistor. The two kinds of the first conductive **ions** are **P** and Ar **ions** . The second conductive **ions** are Ar, **P** , or Sb for forming a **PMOS** transistor; or B or BF2 for forming an **NMOS** transistor.

ELECTRONICS - Preferred Process: The second insulating layer is formed by liquid phase deposition (LPD) of oxide (33) at 25-300 degreesC to a thickness of 500-3,000 Angstrom. The self-aligned silicide layer is formed by:

(a) forming a metal layer on the dielectric spacers, on the first poly-gate and on the second insulating layer;

(b) performing a silicidation annealing; and

(c) etching away any unreacted metal layer.

The silicidation and thermal annealing are performed by a rapid thermal process (RTP) at 350-700 degreesC and 700-1,150 degreesC, respectively, in nitrogen ambient. Preferred Conditions: The first **ion** implantation is carried out at 5-100 keV and at a dose of 5x10power12-1x10power14/cm2. The second **ion** implantation is carried out at 20-120 keV at a dose of at most 5x10power11-1x10power13/cm2, and at a tilted angle of 10-60 degrees.

Preferred Component: The doped region beneath the second polygate has a larger **ion** concentration than a second anti- **punch through** region in the ESD protective region. The phosphoric and arsenic implantations are carried out both at 5-150 keV, and at a dose of 2x10power14-2x10power15/cm2 and 5x10power14-5x10power15/cm2, respectively.

Title Terms: FABRICATE; METAL; OXIDE; SEMICONDUCTOR; TRANSISTOR; ELECTROSTATIC; DISCHARGE; PROTECT; TRANSISTOR; SILICON; SUBSTRATE; FORMING; SILICIDE; LAYER; ULTRA; SHALLOW; JUNCTION; DOUBLE; DIFFUSION; DRAIN; JUNCTION

Derwent Class: L03; U11; U12; U13

International Patent Class (Main): H01L-021/8238

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C02; L04-C10F; L04-E01B

Manual Codes (EPI/S-X): U11-C18A3; U12-D02A9; U13-E01

?

?t s21/9/1

21/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008306116 **Image available**
WPI Acc No: 1990-193117/199025
Related WPI Acc No: 1989-309000
XRPX Acc No: N90-150256

Voltage threshold setting method for power MOSFET **- uses substrate having three layers of differing conductivity and anisotropically etched groove**

Patent Assignee: GEN INSTR CORP (GENN)
Inventor: EINTHOVEN W G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4929987	A	19900529	US 89358883	A	19890530	199025	B

Priority Applications (No Type Date): US 89358883 A 19890530; US 88150755 A 19880201

Abstract (Basic): US 4929987 A

The wafer with a 100 orientation comprises N layer (middle layer) and a lightly doped P layer (top layer). A strongly doped N layer (source layer) is diffused into most of the top layer. An oxide layer is grown. A V groove with a flat bottom is anisotropically etched through openings in the oxide layer. The V groove is etched through the source layer and most of the P layer. The bottom of the groove initially is at a level above the junction between the top layer and the middle layer. Exposure to beam of **phosphorus ions** forms a **shallow** implanted **channel** region proximate the walls of the groove. An unwanted implanted region along the bottom of the groove is also formed.

A second anisotropic etch, through the same oxide mask, deepens the groove bottom to a point below the junction, removing the unwanted portion of the implanted region along the groove bottom. The implanted concentration of the channel is later reduced as the gate oxide is formed. This method of groove formation can be used to set the threshold voltage of enhancement mode power **MOSFETS** .

ADVANTAGE - Provides method for setting threshold voltage without compromising other parameters. Can also be used to produce depletion mode power **MOSFETS** with zero-gate **on resistance** values of a few MILLI-OHM CM(2).

Dwg.4/4

Title Terms: VOLTAGE; THRESHOLD; SET; METHOD; POWER; **MOSFET** ; SUBSTRATE; THREE; LAYER; DIFFER; CONDUCTING; ANISOTROPE; ETCH; GROOVE
Derwent Class: U12
International Patent Class (Additional): H01L-029/78
File Segment: EPI
Manual Codes (EPI/S-X): U12-D02A; U12-E01
?

?t s25/9/1,2,8

25/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04316429
INSULATED GATE TYPE FIELD EFFECT TRANSISTOR

PUB. NO.: 05-308129 [JP 5308129 A]
PUBLISHED: November 19, 1993 (19931119)
INVENTOR(s): KATO JURI
IWAMATSU SEIICHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-345344 [JP 91345344]
FILED: December 26, 1991 (19911226)
INTL CLASS: [5] H01L-027/092
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 1513, Vol. 18, No. 109, Pg. 107, February 22, 1994 (19940222)

ABSTRACT
PURPOSE: To obtain a **CMOS** type semiconductor device whose gate channel length is smaller than or equal to a specified value, by using lamp heating anneal.

CONSTITUTION: In the conventional process, annealing after Pch source.drain formation (sup 11)B ion implantation and Nch source.drain formation (sup 31) **P ion implantation** is performed by N(sub 2) thermal diffusion aneal (II). On the other hand, a surface layer is annealed for several seconds by lamp heating (I). Hence in an insulated gate type field effect transistor which constitutes an integrated circuit and whose main impurities are baron, a transistor composed of impurity diffusion layers of a source and a drain wherein the gate **channel** length is **2 . mu** .m or shorter, the impurity diffusion layer thickness is 0.5.mu.m or smaller, and the sheet resistance is 27.omega./sq or smaller can be reallized. Thereby a **CMOS** type semiconductor device whose gate **channel** length is **2 . mu** .m or shorter can be obtained.

25/9/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03048167 **Image available**
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 02-023667 [JP 2023667 A]
PUBLISHED: January 25, 1990 (19900125)
INVENTOR(s): IWAMATSU SEIICHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-174125 [JP 88174125]
FILED: July 12, 1988 (19880712)
INTL CLASS: [5] H01L-029/784
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 912, Vol. 14, No. 168, Pg. 13, March 30, 1990 (19900330)

ABSTRACT
PURPOSE: To eliminate the long-term variations of threshold voltage due to trapping of hot electrons even when trench depth is made shallow in a trench gate **MOS FET** by forming a drain impurity diffusion layer on source and drain impurity diffusion layers as a double layer structure

composed of high and low concentration layers.

CONSTITUTION: 0.5.mu.m deep, 0.1.mu.m wide trench is formed in a surface of a Si substrate 1. A 50 angstroms -100 angstroms thick gate electrode 3 comprising an SiO(sub 2) film and the like is formed on the side wall of the trench. Additionally, a gate electrode 3 comprising CVD polycrystalline Si and the like is formed on the surface of the film 2 as a gate 7. Low concentration n(sup -) layers 5, 5' are formed into 0. **2** . **mu** .m depth in **source** and drain regions by **ion** - **implantation** of **phosphorus** or arsenic as a source 6 and a drain 8. There is produced hot electrons in the vicinity of the drain owing to the improvement of electric field intensity. Hereby, there is not lowered long-term reliability owing to variations of threshold voltage.

25/9/8 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010009363
WPI Acc No: 1994-277074/199434
XRAM Acc No: C94-126617
CMOS **mfr. giving improved latch-up - using buried oxidn. epitaxy (BOE) by forming oxide film mask, and buried layers resulting in high punch-through voltage**
Patent Assignee: GOLDSTAR ELECTRON CO LTD (GLDS)
Inventor: KIM H; LEE K; SHIN B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 9308900	B1	19930916	KR 9014498	A	19900913	199434	B

Priority Applications (No Type Date): KR 9014498 A 19900913
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 9308900	B1			H01L-027/08	

Abstract (Basic): KR 9308900 B

The **CMOS** is prepd. by forming a oxide film as mask for producing P+ and N+ buried layers on the substrate, implanting 1.0E14-1.0E15 ion and 35 kev - 20 kev energy to form the **P** + buried layer, **implanting** at the same condition to form the N+ buried layer, depositing 1-5 micron epitaxial layer on the all area of the substrate and driving in the implanted ions to reach 0. **3** -0.5 **micron** of the device-surface **channel** .

ADVANTAGE - The device has a high punch-through voltage and an improve latch-up and a good isolation
Title Terms: **CMOS** ; MANUFACTURE; IMPROVE; LATCH-UP; BURY; OXIDATION; EPITAXIAL; FORMING; OXIDE; FILM; MASK; BURY; LAYER; RESULT; HIGH; PUNCH; THROUGH; VOLTAGE
Index Terms/Additional Words: BOE
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-027/08
International Patent Class (Additional): H01L-027/06
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02B
Manual Codes (EPI/S-X): U11-C08A2; U13-D02A
?

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?ds

Set     Items   Description
S1     266683   MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR -
             VMOS? OR DMOS? OR METAL()OXIDE()SEMICONDUTOR?()FIELD()EFFECT(-
             )TRANSISTOR?
S2      28075   CC='B2560R'  Insulated gate field effect transistors
S3     275317   S1 OR S2
S4      18844   PHOSPHORUS(3N)ION? OR P(3N)ION?
S5        569   S4 AND S3
S6       1519   PUNCHTHROUGH?
S7         10   S6 AND S5
S8          9   RD (unique items)
S9       3416   400(2N)KEV OR FOUR()HUNDRED(2N)KEV
S10         2   S5 AND S9
S11      7861   200(2N)KEV OR TWO()HUNDRED(2N)KEV
S12         3   S11 AND S5
S13      6971   RDSON OR ON()RESISTANCE
S14         9   S13 AND S5
S15         6   RD (unique items)
S16   2873001   (SOURCE? OR CHANNEL?)
S17    736940   (ONE OR 1 OR TWO OR 2 OR THREE OR 3) (3N) (MICRON? OR MU OR
              MU()MICRON? OR MICROMETER? OR MICROMETRE?)
S18     11313   S17(5N)S16
S19         8   S18 AND S5
S20         5   RD (unique items)
S21         7   S16 (3N) (DEEP? OR DEPTH?) AND S5
S22         6   RD (unique items)
S23      4456   S16 (3N) SHALLOW?
S24         5   S23 AND S5
?show files
File   2:INSPEC 1969-2002/Sep W3
         (c) 2002 Institution of Electrical Engineers
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         (c) 2002 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2002/Sep W3
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File  34:SciSearch(R) Cited Ref Sci 1990-2002/Sep W3
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         (c) 2002 BLDSC all rts. reserv.
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         (c) 2002 Cambridge Sci Abs
File  94:JICST-EPlus 1985-2002/Jul W3
         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Aug
         (c) 2002 The HW Wilson Co.
File 108:AEROSPACE DATABASE 1962-2002/Aug
         (c) 2002 AIAA
File 144:Pascal 1973-2002/Sep W3
         (c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Aug
         (c) 2002 Cambridge Scient. Abstr
File 305:Analytical Abstracts 1980-2002/Aug W4
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Jul
         (c) 2002 DECHEMA
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Set     Items   Description
S1      266683   MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR -
             VMOS? OR DMOS? OR METAL()OXIDE()SEMICONDUTOR?()FIELD()EFFECT(-
             )TRANSISTOR?
S2       28075   CC='B2560R'  Insulated gate field effect transistors
S3      275317   S1 OR S2
S4       18844   PHOSPHORUS(3N)ION? OR P(3N)ION?
S5         569   S4 AND S3
S6        1519   PUNCHTHROUGH?
S7          10   S6 AND S5
S8           9   RD (unique items)
S9        3416   400(2N)KEV OR FOUR()HUNDRED(2N)KEV
S10          2   S5 AND S9
S11       7861   200(2N)KEV OR TWO()HUNDRED(2N)KEV
S12          3   S11 AND S5
S13       6971   RDSON OR ON()RESISTANCE
S14          9   S13 AND S5
S15          6   RD (unique items)
S16          0   METAL)OXIDE()SEMICONDUCTOR?()FIELD()EFFECT()TRANSISTOR?
S17       6337   METAL()OXIDE()SEMICONDUCTOR?()FIELD()EFFECT()TRANSISTOR?
S18     267711   S17 OR S1
S19      86362   FIELD()EFFECT()TRANSISTOR?
S20     326511   S19 OR S18
S21     331925   S2 OR S20
S22        700   S21 AND S4
S23         11   S22 AND S6
S24         10   RD (unique items)
S25          1   S24 NOT S8
S26          2   S22 AND S9
S27          0   S26 NOT S10
S28          3   S22 AND S11
S29          9   S13 AND S22
S30    2873001   SOURCE? OR CHANNEL?
S31        758   S20 (3N)SHALLOW?
S32          6   S31 AND S22
S33          6   RD (unique items)
?show files
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         (c) 2002 Institution of Electrical Engineers
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         (c) 2002 Cambridge Sci Abs
File  94:JICST-EPlus 1985-2002/Jul W3
         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Aug
         (c) 2002 The HW Wilson Co.
File 108:AEROSPACE DATABASE 1962-2002/Aug
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File 144:Pascal 1973-2002/Sep W3
         (c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Aug
         (c) 2002 Cambridge Scient. Abstr
File 305:Analytical Abstracts 1980-2002/Aug W4
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Jul
         (c) 2002 DECHEMA
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?t s20/9/1-5

20/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4750423 INSPEC Abstract Number: B9410-2560R-049
Title: Temperature and channel-length dependence of impact ionization **in p -channel** MOSFETs
Author(s): Mastrapasqua, M.; Bude, J.; Pinto, M.; Manchanda, L.; Lee, K.F.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
p.125-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xv+168 pp.
ISBN: 0 7803 1921 4
U.S. Copyright Clearance Center Code: 0 7803 1921 4/94/$3.00
Conference Title: Proceedings of 1994 VLSI Technology Symposium
Conference Date: 7-9 June 1994 Conference Location: Honolulu, HI, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: The impact **ionization** (II) current of **p - channel MOSFETs** designed for 0. **1 mu** m operation has been investigated as a function of temperature and channel length, L/sub ch/ down to 0.1 mu m. It has been experimentally observed that at any channel length, the substrate current to source current ratio, I/sub R/, decreases with decreasing lattice temperature. The temperature behavior of the II multiplication measured here is opposite to that in bulk. Such a temperature dependence of I/sub R/, has been already observed for n- **MOSFETs** but, to our knowledge, has never been reported in p- **MOSFETs** . Also, the minimum drain bias for which II is observed is V/sub DS/=1.3 V for the 0.1 mu m p- **MOSFET** devices, which is substantially higher than that observed in deep sub-micron n- **MOSFETs** . Furthermore, I/sub R/ is found to increase with decreasing L/sub ch/. Insight into the physical mechanisms behind these phenomena is given through full band Monte Carlo simulations. (9 Refs)
Subfile: B
Descriptors: digital simulation; impact ionisation; insulated gate field effect transistors; Monte Carlo methods; semiconductor device models
Identifiers: channel-length dependence; temperature dependence; p-channel **MOSFETs** ; impact ionization current; lattice temperature; impact ionisation multiplication; minimum drain bias; deep submicron **PMOSFET** ; full band Monte Carlo simulations; 0.1 micron; 1.3 V
Class Codes: **B2560R** (Insulated gate field effect transistors); B0240G (Monte Carlo methods); B2560B (Modelling and equivalent circuits
Numerical Indexing: size 1.0E-07 m; voltage 1.3E+00 V

20/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4479354 INSPEC Abstract Number: B9310-2560R-048
Title: The study of the charge carriers mobility degradation in the MOS **-transistor channel by means of Hall current**
Author(s): Dostanko, A.P.; Ivkin, V.M.; Salnikova, I.P.
Author Affiliation: Minsk Radioeng. Inst., Byelorussia
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1783 p.590-9
Publication Date: 1992 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 0962 6/92/$4.00
Conference Title: International Conference on Microelectronics: Microelectronics '92
Conference Sponsor: SPIE; IEEE
Conference Date: 21-23 Sept. 1992 Conference Location: Warsaw, Poland
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: The influence of doping the gated oxide of submicron (**channel**

length approximately 2 **mu** m) **MOSFETs** with phosphorus on their characteristic degradation has been investigated. It is shown that **phosphorus** **ion** implantation into polysilicon lying on the oxide in the range of 500-1.500 mu C/cm/sup 2/ followed by thermal treatment at 850 degrees C for diffusing the phosphorus into the oxide results in a negligible threshold voltage growth and transconductance reduction. Mobility degradation in a MOSFET channel of a split drain-contact transistor has been tested by means of an in-situ Hall current method. It is shown that doping oxide with phosphorus leads to a negligible reduction of charge carrier mobility. Device degradation in electric regimes, providing injection of hot carriers into the gated oxide, has been providing injection of hot carriers into the gated oxide, has been studied. (10 Refs)

Subfile: B

Descriptors: carrier mobility; Hall effect; hot carriers; insulated gate field effect transistors; semiconductor device testing; semiconductor doping

Identifiers: submicron **MOSFET** ; **CMOS** ; VLSI; hot carrier degradation; charge carriers mobility degradation; Hall current; influence of doping; gated oxide; polysilicon; thermal treatment; split drain-contact transistor ; injection of hot carriers; Si:P; Si:P-SiO/sub 2/:P

Class Codes: **B2560R** (Insulated gate field effect transistors); B2550B (Semiconductor doping

Chemical Indexing:

Si:P sur - Si sur - P sur - Si:P bin - Si bin - P bin - Si el - P el - P dop (Elements - 1,1,2)

Si:P-SiO2:P int - SiO2:P int - Si:P int - SiO2 int - O2 int - Si int - O int - P int - SiO2:P ss - SiO2 ss - O2 ss - Si ss - O ss - P ss - Si:P bin - SiO2 bin - O2 bin - Si bin - O bin - P bin - Si el - P el - P dop (Elements - 1,1,2,2,1,3,3)

20/9/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

03687467 INSPEC Abstract Number: B90055457

Title: Study of hot-carrier effect in short channel DD MOSFET

Author(s): Yang Zhaomin; Xu Jiasheng

Author Affiliation: Inst. of Microelectron., Qinghua Univ., Beijing, China

Journal: Chinese Journal of Semiconductors vol.10, no.7 p.489-96

Publication Date: July 1989 Country of Publication: China

CODEN: PTTPDZ ISSN: 0253-4177

Language: Chinese Document Type: Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: As- **P** double **ion** -implanted N- **MOSFETs** with **1** **mu** m effective **channel** length were fabricated and investigated. By using process and device simulations, the process was computed and optimized. The simulations are in good agreement with experiment. The results showed that hot-carrier effects in DD **MOSFETs** are weaker than normal ones which have the effective channel length as former. (7 Refs)

Subfile: B

Descriptors: hot carriers; insulated gate field effect transistors; semiconductor device models

Identifiers: semiconductor; hot-carrier effect; short channel DD **MOSFET** ; double ion-implanted; channel length; device simulations

Class Codes: **B2560R** (Insulated gate field effect transistors); B2560B (Modelling and equivalent circuits

Chemical Indexing:

As int - P int - As ss - P ss - As el - P el - As dop - P dop (Elements - 2)

20/9/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

01897938 INSPEC Abstract Number: B82041157, C82031830

Title: **Three-dimensional simulation of VLSI** MOSFETs **: the three-dimensional simulation program WATMOS**
Author(s): Husain, A.; Chamberlain, S.G.
Author Affiliation: Electrical Engng. Dept., Univ. of Waterloo, Waterloo, Ont., Canada
Journal: IEEE Transactions on Electron Devices vol.ED-29, no.4 p. 631-8
Publication Date: April 1982 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Describes a computer simulation program based on a three-dimensional model for small-geometry **MOSFETs** . The effect of Si-SO/sub 2/ interface charge, ion implantation in the channel, **p** /sup +/ isolation field **ion** implant (channel isolations), and shape of the field oxide are all included in the model. The simulations revealed a new insight into VLSI **MOSFET** devices. Some of these results include 'wedge-like' effective channel width, the effective channel width under certain bias conditions decreases to 63 percent of its nominal value. Saddle point related to punchthrough current locus; the punchthrough current per unit width as a function of the channel width was found for the first time to decrease rapidly as the channel width was reduced below 5 mu m. A decrease of punchthrough current by three orders of magnitude was observed as the **channel** width was reduced from **2** to 1k **mu** m. The breakdown voltage of small-geometry devices increases as the channel width decreases. Subthreshold current, potential and electric field distributions, and threshold voltage are significantly different from those calculated using two-dimensional analysis. (25 Refs)
Subfile: B C
Descriptors: field effect integrated circuits; insulated gate field effect transistors; large scale integration; semiconductor device models
Identifiers: subthreshold current; potential distribution; WATMOS; computer simulation program; three-dimensional model; effect of Si-SO/sub 2/ interface charge; ion implantation; **p** /sup +/ isolation field **ion** implant; VLSI **MOSFET** ; effective channel width; punchthrough current locus ; breakdown voltage; small-geometry devices; electric field distributions; threshold voltage
Class Codes: B2560B (Modelling and equivalent circuits); **B2560R** (Insulated gate field effect transistors); B2570F (Other MOS integrated circuits); C7410D (Electronic engineering

20/9/5 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02997548 Genuine Article#: MV678 Number of References: 11
Title: SIGNIFICANCE OF CHARGE SHARING IN CAUSING THRESHOLD VOLTAGE ROLL-OFF IN HIGHLY DOPED 0.1-MU-M SI METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS AND ITS SUPPRESSION BY ATOMIC LAYER DOPING
Author(s): NODA H; NAKAMURA K; KIMURA S
Corporate Source: HITACHI LTD,CENT RES LAB,1-280 HIGASHI KOIGAKUBO/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1994, V33, N1B (JAN), P599-605
ISSN: 0021-4922
Language: ENGLISH Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: PHYSICS, APPLIED
Abstract: An investigation into the influence of substrate doping concentration on the short channel effects in 0.1-mu m **nMOSFETs** (n-channel metal oxide semiconductor field effect transistors) has shown that, when substrate dopant concentration is higher than 1 x 10(18) cm(-3), threshold voltage (V-th) roll-off is not improved by heavier doping in the substrate, although punchthrough is suppressed. Furthermore, it was found that threshold voltage roll-off is characterized by a reduction in subthreshold swing. Experimental

results suggest that the threshold voltage roll-off is heavily influenced by the effect of the two-dimensional shape of the drain depletion region, namely the charge sharing mechanism. As a candidate device for suppressing charge sharing, the ALD (atomic-layer doped) **MOSFET** was considered. Its excellent scalability was demonstrated by device simulation.

Descriptors--Author Keywords: SI ; **MOSFET ;** 0. **1** **MU** -M ; SHORT **CHANNEL** EFFECT ; THRESHOLD VOLTAGE ROLL-OFF ; PUNCHTHROUGH ; CHARGE SHARING ; ALD

Research Fronts: 92-1071 001 (ULTRA SHALLOW JUNCTION FORMATION USING DIFFUSION; SI SUBSTRATE RAPID THERMAL ANNEALING; THIN TI FILMS; IMPLANTING BF2+ **IONS** ; **P** + IMPLANTATION)

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22/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5450398 INSPEC Abstract Number: B9701-2560R-072

Title: Improvement of deep **submicron buried-** channel **p-** MOSFET **by As and P co-implantation for punchthrough stopper**

Author(s): Jeonghwan Son; Sangdon Lee; Kijae Huh; Jeongmo Hwang
Author Affiliation: ULSI Lab., LG Semicon Co. Ltd., Cheongju, South Korea

Conference Title: 1996. 54th Annual Device Research Conference Digest (Cat. No.96TH8193) p.18-19
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 202 pp.
ISBN: 0 7803 3358 6 Material Identity Number: XX96-02784
Conference Title: 1996 54th Annual Device Research Conference Digest
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 24-26 June 1996 Conference Location: Santa Barbara, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)

Abstract: We have demonstrated the buried-channel p- **MOSFET** which is co-implanted with As and **P** **ion** as a punchthrough stopper. It is confirmed that the short-channel effect and the drive current were significantly improved by using this simple process. It is promising for deep submicron n/sup +/-poly single gate **CMOS** . (4 Refs)

Subfile: B
Descriptors: arsenic; ion implantation; **MOSFET** ; phosphorus
Identifiers: **deep** submicron buried- **channel** p- **MOSFET** ; punchthrough stopper; short-channel effect; drive current; n/sup +/-poly single gate **CMOS** ; co-implantation; Si:As,P
Class Codes: **B2560R** (Insulated gate field effect transistors); B2550B (Semiconductor doping
Chemical Indexing:
Si:As,P int - As int - Si int - P int - Si:As,P ss - As ss - Si ss - P ss - As el - Si el - P el - As dop - P dop (Elements - 1,1,1,3)

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24/9/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07358781 Genuine Article#: 155EV Number of References: 9
Title: Arsenic and phosphorus **double** ion **implanted source/drain junction for 0.25- and sub-0.25-mu m** MOSFET **technology**
Author(s): Lee HD (REPRINT) ; Lee YJ
Corporate Source: LG SEMICON CO LTD,R&D DIV, DEVICE TEAM/CHEONGJU 361480//SOUTH KOREA/ (REPRINT)
Journal: IEEE ELECTRON DEVICE LETTERS, 1999, V20, N1 (JAN), P42-44
ISSN: 0741-3106 Publication date: 19990100
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Geographic Location: SOUTH KOREA
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: Arsenic and phosphorus double implanted source/drain junction is proposed for 0.25- and sub-0.25-mu m **NMOSFET** technology, Arsenic is for a shallow high concentration region beneath the silicide and phosphorus is for a slightly deeper junction to increase junction quality and to reduce junction capacitance. The arsenic and phosphorus double implantation is performed after formation of sidewall. The double implanted source/drain junction shows drastic reduction of reverse leakage current and little effect on the short channel characteristics compared with an arsenic only implanted device. Moreover, the circuit performance is improved about 2.5%.
Descriptors--Author Keywords: double ion implantation ; **shallow** junction ; **source** /drain junction ; sub-0.25-mu m **MOSFET**
Identifiers--KeyWord Plus(R): DESIGN
Cited References:
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LEE HD, 1998, V45, P1848, IEEE T ELECTRON DEV
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?t s24/9/2,3,5

24/9/2 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03530578 Genuine Article#: PK410 Number of References: 17
Title: SHORT-CHANNEL CHARACTERISTICS OF SI MOSFET **WITH EXTREMELY** SHALLOW SOURCE **AND DRAIN REGIONS FORMED BY INVERSION-LAYERS**
Author(s): NODA H; MURAI F; KIMURA S
Corporate Source: HITACHI LTD,CENT RES LAB/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1994, V41, N10 (OCT), P 1831-1836
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; PHYSICS, APPLIED
Abstract: The influence of extremely **shallow source** and drain junctions on the short channel effects of Si **MOSFET** 's are experimentally investigated. These extremely shallow junctions are realized in **MOSFET** 's with a triple-gate structure. Two subgates formed as side-wall spacers of a main gate induce inversion layers which work as the virtual source and drain. Significant improvement in threshold voltage roll-off and punchthrough characteristics are obtained in comparison with conventional **MOSFET** 's whose junctions are formed by ion implantation: threshold voltage roll off is suppressed down to a physical gate length of 0.1 mum while punchthrough is suppressed down to 0.07 mum, the minimum pattern size delineated. It is also demonstrated experimentally that the carrier concentrations in the source and drain do not have any influence on the short channel effects.
Research Fronts: 92-1071 001 (ULTRA SHALLOW JUNCTION FORMATION USING DIFFUSION; SI SUBSTRATE RAPID THERMAL ANNEALING; THIN TI FILMS; IMPLANTING BF2+ **IONS** ; **P** + IMPLANTATION)
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24/9/3 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02935806 Genuine Article#: MR536 Number of References: 8
Title: SIMULTANEOUS SHALLOW-JUNCTION FORMATION AND GATE DOPING P-CHANNEL METAL-SEMICONDUCTOR-OXIDE FIELD-EFFECT TRANSISTOR PROCESS USING COBALT SILICIDE AS A DIFFUSION DOPING SOURCE
Author(s): CHEN WM; LIN JP; BANERJEE SK; LEE JC
Corporate Source: UNIV TEXAS,DEPT ELECT & COMP ENGN,MICROELECTR RES CTR/AUSTIN//TX/78712
Journal: APPLIED PHYSICS LETTERS, 1994, V64, N3 (JAN 17), P345-347

ISSN: 0003-6951
Language: ENGLISH   Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: PHYSICS, APPLIED
Abstract: Submicron p-metal-semiconductor-oxide field-effect transistors (**MOSFETs**) have been fabricated using cobalt silicide as a diffusion **source** for forming **shallow** p-n junctions and as a doping source for undoped as-deposited amorphous silicon gate (SADDS). The thermal stability of CoSi2 on polycrystalline silicon is shown to be significantly improved by using as-deposited amorphous silicon instead of as-deposited polycrystalline silicon as the gate material. The p-**MOSFETs** fabricated using the SADDS process exhibit excellent characteristics and open up the possibility of eliminating several masks and implants in more complicated complimentary metal-oxide semiconductor processes.
Identifiers--KeyWords Plus: LEAKAGE
Research Fronts: 92-1071 002   (ULTRA SHALLOW JUNCTION FORMATION USING DIFFUSION; SI SUBSTRATE RAPID THERMAL ANNEALING; THIN TI FILMS; IMPLANTING BF2+ **IONS** ; **P** + IMPLANTATION)
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24/9/5   (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14128609   PASCAL No.: 99-0324736

Dual-workfunction gate engineering in a corner parasitics-free shallow-trench-isolation complementary-metal-oxide-semiconductor technology

SCHWALKE Udo; FULDNER Marc; ZATSCH Walter; BOTHE Katja; HADAWI Dariusch; JANSSEN Ingold; SCHON Peter
Siemens Corporate Technology, 81730 Munich, Germany; Siemens Semiconductor Division, 81730 Munich, Germany
Journal: Japanese Journal of Applied Physics, Part I : Regular papers, short notes & review papers, 1999-04, 38 (4B) 2232-2237
ISSN: 0021-4922   CODEN: JAPNDE   Availability: INIST-9959
Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
Country of Publication: United States
Language: English
In this work, through-the-gate implantation (TGI) of channel- and well-doping is favorably combined with n SUP + /p SUP + gate implantation. This approach offers an additional degree of freedom to optimize dual-workfunction gates independently from the fabrication of ultra- **shallow** **source** /drain junctions. By using the same masks for each device type, no increase in process complexity occurs. In combination with the extended trench isolation gate technology (EXTIGATE) process architecture, a corner parasitics-free shallow trench isolation (STI) is provided together with the separation of pre-implanted n SUP + /p SUP + polySi areas to inhibit lateral n SUP + /p SUP + cross-diffusion during gate activation. Nitrogen co-implantation into the gate is implemented to suppress boron penetration and to provide relief from residual impurity cross-diffusion within the gate during S/D anneals. Besides high drive currents, excellent short channel-behavior and improved narrow width characteristics are obtained with TGI- **CMOS** . (c) 1999 Publication Board, Japanese Journal of Applied Physics.

English Descriptors: Experimental study; Measuring methods; **CMOS** integrated circuits; Integrated circuit technology; Semiconductor doping; **Ion** implantation; Silicon; Boron; **Phosphorus** ; Diffusion; Electrical

properties; Work functions

French Descriptors: 8540R; Etude experimentale; Methode mesure; Circuit integre **CMOS** ; Technologie circuit integre; Dopage semiconducteur; Implantation ion; Silicium; Bore; Phosphore; Diffusion(transport); Propriete electrique; Travail sortie

Classification Codes: 001D03F17

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?t s10/9/1

10/9/1 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0610380 NTIS Accession Number: AD-823 775/2/XAB
Single Crystal Silicon Films on Insulating Substrates (Follow on Program)
(Rept. for 1 Aug-31 Oct 67)
Autonetics Anaheim Calif
Corp. Source Codes: 048100
31 Oct 67 36p
Journal Announcement: GRAI7709
Distribution limitation now removed. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Contract No.: NOBSR-93145; XF-02102; 9356

Space charge limited silicon-on-sapphire **MOS** transistors have been fabricated with transconductances of 950 micromhos and voltage amplification factors of 38. Further development has been conducted on diffused bipolar transistors using new masks with 2.5 micron line widths. Processing has started on an integrated circuit which will compare silicon-on-sapphire with an identical circuit in bulk silicon. Development of an extensive **phosphorus ion** injection technology is in progress, to complement the boron ion doping capability previously established. Injection of **phosphorus ions** at energies up to **400 kev** now permits formation of emitter structures in either ion-injected or diffusion-doped p-type base regions in silicon-on-sapphire material. Planar three-layer (bipolar) structures have been formed by sequential injection both of boron and sodium ions and of boron and **phosphorus ions** into appropriately masked samples. The boron ion doping studies at energies up to **400 kev** have been continued in a variety of epitaxial layers.

Descriptors: Semiconducting films; *Crystal growth; *Silicon; *Integrated circuits; Substrates; Sapphire; Doping; Boron; **Phosphorus** ; **Ions** ; Injection; Transistors; Microstructure; Electron diffraction
Identifiers: Metal oxide transistors; NTISDODXD
Section Headings: 49G (Electrotechnology--Resistive, Capacitive, and Inductive Components); 49B (Electrotechnology--Circuits)
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A novel substrate hot electron and hole injection structure with a double-implanted buried-channel MOSFET

- Yoon, S. Siergiej, R. White, M.H.
Sherman Fairchild Center, Lehigh Univ., Bethlehem, PA, USA

This paper appears in: **Electron Devices, IEEE Transactions on**
On page(s): 2722
Boulder, CO, USA
Dec. 1991
Volume: 38 Issue: 12
ISSN: 0018-9383
References Cited: 3
CODEN: IETDAI
INSPEC Accession Number: 4093083

Abstract:
Summary form only given. Substrate hot electron and hole injection into the same gate insulator is achieved with a double ion-implanted buried-channel n-channel MOSFET device. Under the gate, the impurity profile is n-on-n/sup +/ on a p substrate. The n-on-n/sup +/ buried channel, which is formed by implanting the phosphorus ions twice (first, deep heavy implant and, second, shallow and light implant), makes it possible to inject hot electrons in the accumulation region and hot holes in the inversion region of the device operation. For the case of electron injection, a forward-biased diode adjacent to the stressed device supplies the electrons into the junction space-charge layer between n/sup +/ and p bulk (source and drain are grounded and bulk is held at a large negative voltage). For the case of hot hole injection, the gate is biased to provide a hole inversion layers at the interface.

Index Terms:
substrate hot electron injection substrate hot hole injection shallow light implant double-implanted buried-channel MOSFET gate insulator ion-implanted n-channel impurity profile n-on-n/sup +/ buried channel deep heavy implant accumulation region inversion region forward-biased diode junction space-charge layer hole inversion layers Si:P hot carriers insulated gate field effect transistors ion implantation

?t s7/9/2,3,4

7/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

01897938 INSPEC Abstract Number: B82041157, C82031830
Title: Three-dimensional simulation of VLSI MOSFETs **: the three-dimensional simulation program WATMOS**
Author(s): Husain, A.; Chamberlain, S.G.
Author Affiliation: Electrical Engng. Dept., Univ. of Waterloo, Waterloo, Ont., Canada
Journal: IEEE Transactions on Electron Devices vol.ED-29, no.4 p. 631-8
Publication Date: April 1982 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Describes a computer simulation program based on a three-dimensional model for small-geometry **MOSFETs** . The effect of Si-SO/sub 2/ interface charge, ion implantation in the channel, **p** /sup +/ isolation field **ion** implant (channel isolations), and shape of the field oxide are all included in the model. The simulations revealed a new insight into VLSI **MOSFET** devices. Some of these results include 'wedge-like' effective channel width, the effective channel width under certain bias conditions decreases to 63 percent of its nominal value. Saddle point related to **punchthrough** current locus; the **punchthrough** current per unit width as a function of the channel width was found for the first time to decrease rapidly as the channel width was reduced below 5 mu m. A decrease of **punchthrough** current by three orders of magnitude was observed as the channel width was reduced from 2 to 1k mu m. The breakdown voltage of small-geometry devices increases as the channel width decreases. Subthreshold current, potential and electric field distributions, and threshold voltage are significantly different from those calculated using two-dimensional analysis. (25 Refs)
Subfile: B C
Descriptors: field effect integrated circuits; insulated gate field effect transistors; large scale integration; semiconductor device models
Identifiers: subthreshold current; potential distribution; WATMOS; computer simulation program; three-dimensional model; effect of Si-SO/sub 2/ interface charge; ion implantation; **p** /sup +/ isolation field **ion** implant; VLSI **MOSFET** ; effective channel width; **punchthrough** current locus; breakdown voltage; small-geometry devices; electric field distributions; threshold voltage
Class Codes: B2560B (Modelling and equivalent circuits); **B2560R** (Insulated gate field effect transistors); B2570F (Other MOS integrated circuits); C7410D (Electronic engineering

7/9/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04514780 E.I. No: EIP96093347993
Title: Improvement of deep submicron buried-channel p- MOSFET **by As and P co-implantation for** punchthrough **stopper**
Author: Son, Jeonghwan; Lee, Sangdon; Huh, Kijae; Hwang, Jeongmo
Corporate Source: LG Semicon Co, Ltd, Cheongju, S Korea
Conference Title: Proceedings of the 1996 54th Annual Device Research Conference Digest, DRC
Conference Location: Santa Barbara, CA, USA Conference Date: 19960624-19960626
Sponsor: IEEE
E.I. Conference No.: 45352
Source: Annual Device Research Conference Digest 1996. IEEE, Piscataway, NJ, USA. p 18-19
Publication Year: 1996
CODEN: 002334
Language: English

Document Type: CA; (Conference Article) Treatment: X; (Experimental)
Journal Announcement: 9611W4

Abstract: This paper demonstrates the buried-channel p- **MOSFET** which is co-implanted with AS and **P ion** as a **punchthrough** stopper. It is confirmed that the SCE and the drive current were significantly improved by using this simple process. It is promising for deep submicron n** plus -poly single gate **CMOS** . 4 Refs.

Descriptors: **MOSFET** devices; **Ion** implantation; Arsenic; **Phosphorus** ; Gates (transistor); Leakage currents; Semiconductor device manufacture; Ionization; Electric breakdown

Identifiers: Buried channel **pMOSFETs** ; **Punchthrough** stopper; Coimplantation technique; Short channel effect; Drain leakage currents; Impact ionization rate

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 932.1 (High Energy Physics); 701.1 (Electricity: Basic Concepts & Phenomena); 931.2 (Physical Properties of Gases, Liquids & Solids)

714 (Electronic Components); 932 (High Energy, Nuclear & Plasma Physics); 804 (Chemical Products); 701 (Electricity & Magnetism); 931 (Applied Physics)

71 (ELECTRONICS & COMMUNICATIONS); 93 (ENGINEERING PHYSICS); 80 (CHEMICAL ENGINEERING); 70 (ELECTRICAL ENGINEERING)

7/9/4 (Item 2 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

02861478 E.I. Monthly No: EIM9002-005895

Title: Purification of P2** plus beam and anti-punch-through implantation of P-channel** MOSFET **.**

Author: Li, Jin-hua; Pan, Yi-ming
Corporate Source: Shanghai Inst of Metallurgy, China

Conference Title: Proceedings of the International Symposium on Applications of Ion Beams Produced by Small Accelerators
Conference Location: Jinan, China Conference Date: 19871020
Sponsor: High Voltage Engineering Europa BV, Amersfoort, Neth
E.I. Conference No.: 12707
Source: Vacuum v 39 n 2-4 1989. p 209-210
Publication Year: 1989
CODEN: VACUAV ISSN: 0042-207X
Language: English
Document Type: JA; (Journal Article) Treatment: X; (Experimental)
Journal Announcement: 9002

Abstract: A purified P**2** plus beam has been obtained by controlling the source pressure and the source magnet. It has been used for anti-punch-through implantation of P-channel of **CMOS** devices with satisfactory results. The action of the beam filter and the purification mechanism are discussed, and the experimental results are presented. (Edited author abstract) 3 Refs.

Descriptors: ION BEAMS--*Purification; PHOSPHORUS; SEMICONDUCTOR DEVICES, **MOSFET** --Ion Implantation

Identifiers: **CMOSFET** ; **PHOSPHORUS IONS** ; **PUNC HTHROUGH IMP** LANTATION

Classification Codes:

932 (High Energy, Nuclear & Plasma Physics); 714 (Electronic Components)

93 (ENGINEERING PHYSICS); 71 (ELECTRONICS & COMMUNICATIONS)

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?t s12/9/1-3

12/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

02463193 INSPEC Abstract Number: B85035161
Title: High energy ion implantation for CMOS **isolation n-wells technology: problems related to the use of multicharged** phosphorus ions **in an industrial context**
Author(s): Spinelli, P.; Escaron, J.; Soubie, A.; Bruel, M.
Author Affiliation: LETI-IRDI, LETI-CEA, Grenoble, France
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B6, no.1-2 p.283-6
Publication Date: Jan. 1985 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/85/$03.30
Conference Title: Proceedings of the Fifth International Conference on Ion Implantation Equipment and Techniques
Conference Sponsor: IBM
Conference Date: 23-27 July 1984 Conference Location: Jeffersonville, VT, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: It has been shown that high energy ion implantation can be a very attractive technique for producing isolation wells in **CMOS** technology. This technique needs high energy ion implantation equipment which is still rare and expensive, so the use of multicharged ions with a **200 keV** industrial machine could be a good alternate solution. The authors present the results obtained with the spreading resistance technique on beveled samples of silicon which have been implanted with triply charged **phosphorus ions** (600 **keV**), with a **200** DF-4 Extrion machine. They show that the high pressure in the extraction region leads to a molecular decomposition phenomenon and so induces errors into the true implanted dose and the in-depth phosphorus profile. They have observed that these effects can be eliminated when PF/sub 5/ is used as dopant gas in the source instead of PH/sub 3/+H/sub 2/. However, the using of PF/sub 5/ gives rise to a decrease of the filament file. Some spreading-resistance profiles of high energy phosphorus implantations are presented showing a strong channeling effect in the case of a normal incident ion beam. (5 Refs)
Subfile: B
Descriptors: **CMOS** integrated circuits; integrated circuit technology; ion implantation
Identifiers: Si; semiconductor; in depth P profile; **P** /sup 3+/ **ions** ; high energy ion implantation; isolation wells; **CMOS** technology; multicharged ions; spreading resistance technique; beveled samples; 200 DF-4 Extrion machine; high pressure; extraction region; molecular decomposition phenomenon
Class Codes: B2550B (Semiconductor doping); B2570D (CMOS integrated circuits)

12/9/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1189285 NTIS Accession Number: DE85751554
High Energy Ion Implantation for C- MOS **Isolation N-Wells Technology: Some Problems Related to the Use of Multicharged Phosphorous Ions in an Industrial Context**
Spinelli, P. ; Escaron, J. ; Soubie, A. ; Bruel, M.
CEA Centre d'Etudes Nucleaires de Grenoble (France).
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Country of Publication: France
It has been shown that high energy ion implantation can be a very attractive technique for the realisation of isolation wells in C- **MOS** technology. This technique needs high energy ion implantation equipment which is still rare and expensive, so the use of multi-charged ions with a **200** **keV** industrial machine could be a good spare solution. In this paper, we present the results obtained with the spreading resistance technique on beveled samples of silicon which have been implanted with triply charged phosphorous ions (600 **keV**), with a **200** DF-4 extrion machine. We show that the high pressure in the extraction region leads to a molecular decomposition phenomenon and so induces errors on the true implanted dose and on the in-depth phosphorous profile. On one hand, we have observed that these effects can be eliminated when PF sub 5 is used as dopant gas in the source instead of PH sub 3 + H sub 2 . On the other hand the using of PF sub 5 gives rise to a decrease of the filament life. Some spreading-resistance profiles of high energy phosphorous implantations are presented showing a strong channeling effect in case of normal incident ion beam. (ERA citation 10:029001)
Descriptors: **MOS** Transistors; * **Ion** Implantation; * **Phosphorus** **Ions** ; KeV Range 100-1000; Multicharged Ions; Specifications
Identifiers: Foreign technology; * **CMOS** ; ERDA/640301; ERDA/360601; Silicon; Ion sources; NTISDEE
Section Headings: 94G (Industrial and Mechanical Engineering--Manufacturing Processes and Materials Handling); 41E (Manufacturing Technology--Manufacturing, Planning, Processing, and Control); 49H (Electrotechnology--Semiconductor Devices)

12/9/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01778745 E.I. Monthly No: EI8507060261 E.I. Yearly No: EI85102699
Title: HIGH ENERGY ION IMPLANTATION FOR C- MOS **ISOLATION n-WELLS TECHNOLOGY: PROBLEMS RELATED TO THE USE OF MULTICHARGED PHOSPHOROUS IONS IN AN INDUSTRIAL CONTEXT.**
Author: Spinelli, P.; Escaron, J.; Soubie, A.; Bruel, M.
Corporate Source: CEA, Lab d'Electronique et de Technologie de l'Information, Grenoble, Fr
Source: Nuclear Instruments & Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms v B6 n 1-2 Jan 1985, Ion Implant Equip & Techniques, Proc of the 5th Int Conf, Jeffersonville, VT, Jul 23-27 1984 p 283-286
Publication Year: 1985
CODEN: NIMBEU
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications); X; (Experimental)
Journal Announcement: 8507
Abstract: It has been shown that high energy ion implantation can be a very attractive technique for producing isolation wells in C- **MOS** technology. This technique needs high energy ion implantation equipment which is still rare and expensive, so the use of multicharged ions with a **200** **kev** industrial machine could be a good alternate solution. In this paper, the results obtained with the spreading resistance technique on beveled samples of silicon which have been implanted with triply charged phosphorous ions (600 **kev**), with a **200** DF-4 Extrion machine are presented. It is shown that the high pressure in the extraction region leads to a molecular decomposition phenomenon and so induces errors into the true implanted dose and the in-depth phosphorous profile. 5 refs.
Descriptors: SEMICONDUCTOR MATERIALS--*Ion Implantation; **ION** BEAMS; **IONS** ; **PHOSPHORUS**
Identifiers: C- **MOS** ISOLATION; ION ENERGIES; ISOLATION WELLS

Classification Codes:
531 (Metallurgy & Metallography); 712 (Electronic & Thermionic Materials); 932 (High Energy, Nuclear & Plasma Physics); 505 (Mines & Mining, Nonmetallic)
53 (METALLURGICAL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS); 93 (ENGINEERING PHYSICS); 50 (MINING ENGINEERING)
?

15/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5193936 INSPEC Abstract Number: B9604-2560R-017
Title: Thin-film SOI power MOSFET **design based on emission microscopy**
Author(s): Matsumoto, S.; Fukumitsu, T.; Il-Jung Kim; Sakai, T.; Yachi, T.
Author Affiliation: NTT Interdisciplinary Res. Labs, Tokyo, Japan
Conference Title: Proceedings of the 7th International Symposium on Power Semiconductor Devices and ICs, ISPSD `95 (IEEE Cat. No.95CH35785) p. 460-5
Publisher: Inst. Electr. Eng. Japan, Tokyo, Japan
Publication Date: 1995 Country of Publication: Japan xvii+502 pp.
ISBN: 0 7803 2618 0 Material Identity Number: XX95-00956
Conference Title: Proceedings of International Symposium on Power Semiconductor Devices and IC`s: ISPSD `95
Conference Sponsor: Tech. Committee on Electron Devices Inst. Electr. Eng. Japan; IEEE Electron Devices Soc.; Tech. Group on Silicon Devices & Mater. Inst. Electron. Inf. & Commun. Eng. Japan
Conference Date: 23-25 May 1995 Conference Location: Yokohama, Japan
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: We have designed an improved 200-V-class thin-film SOI power **MOSFET** with a stripe-gate topology. A fabricated new device attained a breakdown voltage of 210 V and a specific **on - resistance** of 2.7 Omega .mm/sup 2/. The new device structure is designed based on the results of emission microscopy analysis of the avalanche breakdown points of devices with stripe-gate and cellular-gate topologies. In the standard stripe-gate topology, the avalanche breakdown occurred at the LOCOS edge of the drain offset region. We raised the breakdown voltage by additional **phosphorus ion** implantation at this site. (10 Refs)
Subfile: B
Descriptors: avalanche breakdown; electron microscopy; ion implantation; photoemission; power **MOSFET** ; silicon-on-insulator; thin film transistors
Identifiers: thin-film SOI power **MOSFET** ; emission microscopy; stripe gate; **on - resistance** ; avalanche breakdown; cellular gate; LOCOS; **phosphorus ion** implantation; 200 V
Class Codes: **B2560R** (Insulated gate field effect transistors); B2550B (Semiconductor doping
Numerical Indexing: voltage 2.0E+02 V

15/9/6 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

12076250 PASCAL No.: 95-0278145

Failure analysis and new design of a thin-film silicon-on-insulator power metal-oxide-semiconductor field-effect transistor based on emission microscopy and 2-dimensional device simulation

MATSUMOTO S; FUKUMITSU T; IL-JUNG KIM; SAKAI T; YACHI T
NTT Interdisciplinary Research Laboratories, Musashimo-shi, Tokyo 180, Japan

Journal: Japanese journal of applied physics, 1995, 34 (4A p.1) 1790-1795
ISSN: 0021-4922 CODEN: JJAPA5 Availability: INIST-9959; 354000056393810140
No. of Refs.: 16 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: Japan
Language: English

Thin-film silicon-on-insulator (SOI) power metal-oxide-semiconductor field-effect transistors (**MOSFETs**) with a standard stripe-gate topology and a cellular-gate topology have been fabricated. The breakdown voltage for the stripe-gate topology is half that for the cellular-gate topology-in 200-V-class power **MOSFETs** . Their failure modes are analyzed by emission microscopy and 2-dimensional device simulation for the first time and a new device structure is proposed based on the results of this analysis. The fabricated new device attains a breakdown voltage of 200 V and a specific **on - resistance** of 2.7 OMEGA .mm SUP 2

English Descriptors: Silicon on insulator technology; Power transistor; **MOS** transistor; Field effect transistor; Breakdown voltage; Emission electron microscopy; Theoretical study; Numerical simulation; Two dimensional model; Failure analysis; Structural design; Thin film transistor; Size effect; Ion implantation; Experimental study; Cross section; Electric field gradient; Transistor drain; Voltage current curve ; Thickness; **Phosphorus ion** ; LOCOS technology

French Descriptors: Technologie silicium sur isolant; Transistor puissance; Transistor **MOS** ; Transistor effet champ; Tension amorcage; Microscopie electronique emission; Etude theorique; Simulation numerique; Modele 2 dimensions; Analyse dommage; Calcul construction; Transistor couche mince ; Effet dimensionnel; Implantation ion; Etude experimentale; Coupe transversale; Gradient champ electrique; Drain transistor; Caracteristique courant tension; Epaisseur; Phosphore ion; IPLSI; Intelligent power large scale integration; Stripe gate technology; Technologie LOCOS

Classification Codes: 001D03F05

?t s33/9/4

33/9/4 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03530578 Genuine Article#: PK410 Number of References: 17
Title: SHORT-CHANNEL CHARACTERISTICS OF SI MOSFET **WITH EXTREMELY** SHALLOW **SOURCE AND DRAIN REGIONS FORMED BY INVERSION-LAYERS**
Author(s): NODA H; MURAI F; KIMURA S
Corporate Source: HITACHI LTD,CENT RES LAB/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1994, V41, N10 (OCT), P 1831-1836
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; PHYSICS, APPLIED
Abstract: The influence of extremely shallow source and drain junctions on the short channel effects of Si **MOSFET** 's are experimentally investigated. These extremely shallow junctions are realized in **MOSFET** 's with a triple-gate structure. Two subgates formed as side-wall spacers of a main gate induce inversion layers which work as the virtual source and drain. Significant improvement in threshold voltage roll-off and punchthrough characteristics are obtained in comparison with conventional **MOSFET** 's whose junctions are formed by ion implantation: threshold voltage roll off is suppressed down to a physical gate length of 0.1 mum while punchthrough is suppressed down to 0.07 mum, the minimum pattern size delineated. It is also demonstrated experimentally that the carrier concentrations in the source and drain do not have any influence on the short channel effects.
Research Fronts: 92-1071 001 (ULTRA SHALLOW JUNCTION FORMATION USING DIFFUSION; SI SUBSTRATE RAPID THERMAL ANNEALING; THIN TI FILMS; IMPLANTING BF2+ **IONS** ; **P** + IMPLANTATION)
Cited References:
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YAU LD, 1974, V17, P1059, SOLID STATE ELECTRON
?

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?ds

Set     Items   Description
S1      38550   MOSFET? OR MOS()FET? OR MOS OR CMOS? OR NMOS? OR PMOS? OR -
             VMOS? OR DMOS? OR METAL()OXIDE()SEMICONDUCTOR?()FIELD()EFFECT-
             ()TRANSISTOR?
S2       3256   PHOSPHORUS(3N)ION? OR P(3N)ION?
S3       5804   (ION OR IMPLANT?) (3N) (PHOSPHORUS OR P)
S4       6052   S2 OR S3
S5       2368   S4 AND S1
S6       1619   PUNCHTHROUGH? OR PUNCH()THROUGH? OR WALKOUT? OR WALK()OUT?
S7        393   S6 AND S5
S8        238   S7 AND VERTICAL?
S9        197   400(2N)KEV OR FOUR()HUNDRED(2N)KEV OR 200(2N))KEV OR TWO()-
             HUNDRED(2N)KEV
S10        12   S9 AND S7
S11        42   S9 AND S5
S12      3422   RDSON OR ON()RESISTANCE?
S13        55   S12 AND S7
S14       258   S12 AND S5
S15       180   S14 AND ION?
S16         0   S13 AND L6
S17       338   L13 AND L10
S18        55   S13 AND S6
S19         2   S18 AND S9
S20        34   S18 AND SHALLOW?
S21      1485   (SOURCE? OR CHANNEL?) (5N) (SHALLOW?)
S22        12   S21 AND S18
S23        11   S22 NOT S19
S24    264565   MICRON? OR MU OR MU()MICRON? OR MICROMETER? OR MICROMETRE?
S25        11   S24 AND S23
?show files
File 348:EUROPEAN PATENTS 1978-2002/Sep W02
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020912,UT=20020905
         (c) 2002 WIPO/Univentio
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?t s19/ti,pn,pd,an,ad,au,pa,ae,k/1-2

19/TI,PN,PD,AN,AD,AU,PA,AE,K/1 **(Item 1 from file: 348)**

Low voltage mosfet **with low** on - resistance **and high breakdown voltage**
Wiederspannungs- MOSFET **mit niedrigem Anschaltwiderstand und hoher Durchbruchspannung**
MOSFET **basse tension a faible resistance a l'etat conducteur et haute tension de claquage**

PATENT ASSIGNEE:
SILICONIX Incorporated, (763030), 2201 Laurelwood Road, Santa Clara California 95054, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Williams, Richard K., 10292 Norwich Avenue, Cupertino, CA 95014, (US)
PATENT (CC, No, Kind, Date): EP 779665 A2 970618 (Basic)
EP 779665 A3 971008
APPLICATION (CC, No, Date): EP 96118744 961122;
PRIORITY (CC, No, Date): US 570876 951212

ABSTRACT EP 779665 A2
A low voltage power **MOSFET** is disclosed which includes spaced apart base regions defining a conduction region therebetween. A highly doped region is provided adjacent the conduction region and is spaced from the base regions, being substantially equidistant thereto and extending therebelow. The spacing of the highly doped region from the base regions provides enhanced conductivity of the device and avoids the problem of device breakdown and **punchthrough** in regard to the source regions of the low voltage power device.

Low voltage mosfet **with low** on - resistance **and high breakdown voltage**
Wiederspannungs- MOSFET **mit niedrigem Anschaltwiderstand und hoher Durchbruchspannung**
MOSFET **basse tension a faible resistance a l'etat conducteur et haute tension de claquage**

...ABSTRACT A2
A low voltage power **MOSFET** is disclosed which includes spaced apart base regions defining a conduction region therebetween. A highly...

...regions provides enhanced conductivity of the device and avoids the problem of device breakdown and **punchthrough** in regard to the source regions of the low voltage power device.

SPECIFICATION BACKGROUND OF THE INVENTION
This invention relates to vertical **MOSFET** technology, and more particularly, to vertical **MOSFET** devices which are particularly useful in low voltage applications.

BACKGROUND OF THE INVENTION
In the past, attempts have been made to produce a high power **MOSFET** which combines low **on - resistance** with a reasonably high breakdown voltage. Reference is made, for example, to U.S. Patent...

...assigned to International Rectifier Corporation.
As disclosed therein, and as shown in Fig. 1., a **MOSFET** device 10 includes an N+ silicon substrate 12 having an N- epitaxial layer 14 thereon...

...base regions 16.
While such a device 10 has been found to provide somewhat lower **on resistance** , the doping concentration of the enhanced conductivity region 20 in fact can be increased only...

...a threshold adjust.
However, in application of such a feature to a low voltage power

MOSFET device such as those being used, for example, in disk drives, cellular phones, desktop computers...
...layer, the breakdown along the base region junction with the epitaxial layer will degrade and **punchthrough** might occur between a source region and the heavily doped region, because one is forced...

...low voltage devices.

SUMMARY OF THE INVENTION
In the present invention, a low voltage power **MOSFET** device includes a highly doped enhanced conductivity region which is spaced from and does not...

...conductivity of the device, but with the problem of breakdown along the base junction and **punchthrough** of the device being averted.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view...

...PREFERRED EMBODIMENTS
With reference to Fig. 2, shown therein is a low-voltage, high power **MOSFET** device 40 in accordance with a first embodiment of the invention. Such a device 40...layer 46 without the polysilicon gate electrode 60 in place, in an N channel device, **phosphorus** may be **implanted** in a dose of 1X1014) atoms/cm2) to 5X1015) atoms/cm2) at an energy level in the range of **400** -800 **KeV** . When implanting through the polysilicon gate electrode 60, the appropriate energy level range would be...

...again be 1X1014) atoms/cm2) to 5X1015) atoms/cm2) at an implant energy of 200- **400** **KeV** . In such a device, when implanting through the polysilicon gate electrode, the appropriate range of...

...implant dose and range disclosed has been selected to achieve a noticeable beneficial reduction in **on resistance ,** implanting a lower dose may still show some improvement but with reduced benefit.
The spacing...

...The inclusion of such highly doped region 58 spaced from the base regions 48 decreases **on resistance** of the device 40 and avoids the problem of device breakdown and **punchthrough** in regard to the source regions as described above.
Reference is made to Figs. 3...

...148 implant is undertaken using boron for an N channel device or phosphorus for a **P** channel device. The **implant** is undertaken at a dosage of 1X1013)-1X1014) atoms/cm2) at an energy level of...

...an N+ substrate 80 doped with arsenic or antimony is provided and is masked and **implanted** with **phosphorus ,** and then an epitaxial layer 82 is grown. The substrate 80 and epitaxial layer 82 highly doped region 86 decreases **on resistance** of the device and avoids the problem of device breakdown and **punchthrough** in regard to the source regions as described above, because of the spacing of the...

CLAIMS 1. A high power **metal oxide semiconductor field effect transistor** device comprising:
a semiconductor body having a semiconductor body surface, said semiconductor body being of...

19/TI,PN,PD,AN,AD,AU,PA,AE,K/2 (Item 1 from file: 349)

A SUPER-SELF-ALIGNED TRENCH-GATE DMOS **WITH REDUCED** ON - RESISTANCE
A SUPER-SELF-ALIGNED TRENCH-GATE DMOS **WITH REDUCED** ON - RESISTANCE
Patent Applicant/Inventor:

WILLIAMS Richard K, 10292 Norwich Avenue, Cupertino, CA 95014, US, US (Residence), US (Nationality)
GRABOWSKI Wayne, 1390 Miravalle Avenue, Los Altos, CA 94024, US, US (Residence), US (Nationality)
Patent and Priority Information (Country, Number, Date):
Patent: WO 200065646 A1 20001102 (WO 0065646)
Application: WO 2000US10770 20000421 (PCT/WO US0010770)

English Abstract
A novel super-self-aligned (SSA) structure and manufacturing process uses a single photomasking layer to define critical features and dimensions of a trench-gated vertical power **DMOSFET** . The single critical mask determines the trench surface dimension, the silicon source-body mesa width between trenches, and the dimensions and location of the silicon mesa contact. The contact is self-aligned to the trench, eliminating the limitation imposed by contact-to-trench mask alignment in conventional trench **DMOS** devices needed to avoid process-induced gate-to-source shorts. Oxide step height above the silicon surface is also reduced avoiding metal step coverage problems. Poly gate bus step height is also reduced. Other features described include polysilicon diode formation, controlling the location of drain-body diode breakdown, reducing gate-to-drain overlap capacitance, and utilizing low-thermal budget processing techniques.

A SUPER-SELF-ALIGNED TRENCH-GATE DMOS **WITH REDUCED** ON - RESISTANCE
A SUPER-SELF-ALIGNED TRENCH-GATE DMOS **WITH REDUCED** ON - RESISTANCE
Fulltext Availability:
Detailed Description
Claims

English Abstract
...single photomasking layer to define critical features and dimensions of a trench-gated vertical power **DMOSFET** . The single critical mask determines the trench surface dimension, the silicon source-body mesa width...

...the trench, eliminating the limitation imposed by contact-to-trench mask alignment in conventional trench **DMOS** devices needed to avoid process-induced gate-to-source shorts. Oxide step height above the...

French Abstract
...couche de photoresist unique afin de definir des caracteristiques et des dimensions critiques d'un **DMOSFET** de puissance verticale et a grille a tranchee. Le masque critique unique determine les dimensions...

...qui elimine la limite imposee par l'alignement du masque contact-tranchee dans des dispositifs **DMOS** a tranchee classiques devant eviter des court-circuits entre la grille et la source. La...

Detailed Description
A Super-Self-Aligned Trench-Gate **DMOS**
With Reduced **On - Resistance**
Background
Figure I illustrates a conventional vertical double-diffused **MOSFET** (**DMOS**) IO with a trench gate I 1, a diffused P-type body diffusion (P,,), a...

...short channel, which normally has an effective length of 0.3 to I @tm.

The **on - resistance** of such a device is determined by the sum of its resistive components shown in...

...Rch + Repi + Rsuh
where
Repi = Repil + Repi2 (2)
The primary design goal for a power **MOSFET** used as a switch is to achieve the lowest **on - resistance** by simultaneously minimizing each of

'its resistive constituents. The following factors must be considered.

1...

...is minimized.

3. There is an unavoidable tradeoff between the avalanche breakdown voltage and the **on - resistance** of the device. Higher breakdown voltages require thicker, more lightly doped epitaxial layers contributing higher...

...by maximizing the channel perimeter for a 0 given area. The individual cells of the **MOSFET** may be constructed in any striped or polygonal shape. Ideally, the shape chosen should be...

...a given area. By paralleling many cells and operating them in tandem an extremely low **on - resistance** can be achieved.

5. Higher cell densities have the advantage that the current in the...

...for a given area lowers the channel resistance (Rh) I since the equation for the **MOSFET** channel conduction depends on the total "perimeter" of the gate, not the area of the device.

The equation for the channel resistance of a conventional lateral **MOSFET** can be used 5 to approximate the channel resistance of a vertical **DMOS**
.

I
Rch = (3)
W
Cox
. (VGS - VI)
Lch
where
Cox 6 ox (4)
XOX
combining...

...gate is small compared to the source-body dimension. Since in a conventional trench-gated **DMOS** , manufacturing a small trench is not as difficult as manufacturing a small silicon mesa, the...The presence of a source at the square comers in an array of trench-gated **DMOS** cells has been found to lead to off-state leakage in the device, possibly due...

...The need for comer blocking may conceivably be eliminated in a hexagonal cell trench 0 **DMOS** (see Figure 4D), since the angles around the perimeter of the hexagonal mesas are less...

...Thus, to maximize the cell density and minimize the cell pitch of a vertical trenchgated **DMOS** . the trench gate surface dimension and the surface dimension of the mesa should both be...

...5A-5E illustrate the components of variability in setting the minimum size of the trench **DMOS** mesa. In this case the mesa width is set by three design rules I . Minimum...P+ contact areas. Below this 2 Pm mesa it becomes difficult to implement a trench **DMOS** using a contact mask and a butting N+/P+ source-body contact. In such a...

...dimensions other manufacturing-related problems exist.

Another design and process consideration in a trench-gated **DMOS** is the resistance of the body region P,, and the quality of the body contact...

...forwardbiasing of the emitter-base junction and avoids consequent minority carrier (electron) injection into the **MOSFET** 's body (i.e. base).

The frequency of the body pickup determines the base resistance...

...achieve a low resistance ohmic contact to the body, are specific to each trench-gated **DMOS** design and process. Many commercial power **MOSFETs** today are inadequate in this regard and suffer from snapback and ruggedness problems as a...

...a power device. Surface metal resistance can add milliohms of resistance to a trench-gated **DMOS** laterally (as current flows along the surface of the device to the bond wire or source pickup), producing a significant fractional increase in the **on - resistance** of a large die 0 product. A thick metal layer (e.g. 3 to 4 ...introduce dopants through it.

5 To summarize, one problem with existing conventional trench-gated vertical **DMOS** devices is that the cell density cannot be increased and the geometric-area-to-gate...

...the area efficiency of low-onresistance switches, since the construction of conventional trench-gated vertical **DMOS** -8 imposes fundamental restrictions in cell dimensions. The resistance penalty is especially significant for low...

...where a large portion of the total resistance is attributable to the resistance of the **MOS** channel (Rh). The limitations on cell density are primarily a consequence of the minimum width...

...Summary of the Invention

These problems are solved in a super self-aligned (SSA) trench **DMOSFET** in accordance with this invention. An SSA trench **MOSFET** according to this invention comprises a semiconductor body having a trench formed therein, a wall...

...mesa between segments of the trench can be made smaller than was possible with conventional **MOSFETs** . As explained above, this in turn allows the cell density to be increased and the...

...to conform generally to the shape of the trench gate, is used to reduce the **on - resistance** of the **DMOSFET** . One way of achieving this structure ...is to implant the buried layer after the trenches have been formed.

An SSA trench **MOSFET** is advantageously produced by a process described herein.

The process comprises: providing a body of...

...of the brawings

Figure I illustrates a cross-sectional view of a conventional vertical trench **DMOSFET** .

Figure 2 illustrates a cross-sectional view of a conventional vertical trench **DMOSFET** showing the resistive components of the device. 5 Figures 3A and 3B illustrate cross-sectional views of a conventional vertical trench **DMOSFET** showing the benefit of cell density in improving epitaxial drain spreading resistance.

Figures 4A-4D illustrate plan and cross-sectional views of various trench **DMOS** source geometries. Figure 4A shows a stripe geometry. Figure 4B shows a square cell geometry...

...geometry. '

Figures 5A-5F illustrate the design rules for the mesa of a conventional trench **DMOSFET** . Figure 5A shows the contact-to-trench design rule. Figure 5B shows the contactto-source...

...body. 1 0 Figure 6 illustrates a cross-sectional view of a conventional stripe trench **DMOSFET** with a contact mask feature and with the N+ source extending across the entire mesa...

...and 7C are cross-sectional, plan and perspective views, respectively, of a "ladder"-source trench **DMOS** with contact mask. Figure 8A is a cross-sectional view of a conventional trench **DMOSFET** illustrating the step coverage problem with a conformal thin metal layer.

Figure 8B is a cross-sectional view of a conventional trench **DMOSFET** illustrating the step coverage problem with a thick metal layer.

Figure 8C illustrates the keyhole...

...coverage problem of a metal layer over a polysilicon gate bus in a conventional trench **DMOSFET** .

Figure 9B illustrates a plan view of the intersection of gate trenches in a conventional trench **DMOSFET** .

Figure 9C illustrates a cross-sectional view showing the minimum polysilicon refill thickness in a trench **DMOSFET** .

Figure I OA is a graph showing the equivalent vertical **MOSFET** cell density as a ftinction of mesa width.

Figure I OB is a graph showing the equivalent vertical **MOSFET** cell density as a function of cell pitch. Figures I 1A- I I...

...process sequence for manufacturing a super self-aligned (SSA) source contact in a trench-gated **MOSFET** .

Figures 12A and 12B are cross-sectional views that show the comparison of a **MOSFET** manufactured with a conventional contact mask (Figure 12A) and a **MOSFET** manufactured using the SSA process (Figure 12B). Figure 12C shows a **MOSFET** manufactured by the SSA process but with a contact-maskdefined oxide feature overlying the trench.

Figure 13 is a graph of the vertical **DMOS** cell perimeter ratio A/W as a function of mesa width.

Figure 14 is a graph of the vertical **DMOS** cell perimeter ratio A/W as a function of cell density.

Figures 15A- I 5D are cross-sectional views of various embodiments of a SSA trench **DMOSFET** . Figure 15A shows a full mesa N+ source wherein the P-body is contacted in...

...15B shows an embodiment similar to the one shown in Figure 15A, except that the **MOSFET** includes a deep clamping diode. Figure 15C shows an embodiment similar to the one shown in Figure 15B, except that the **MOSFET** includes a relatively shallow clamping diode. Figure 15D shows an embodiment wherein the source metal...the drain (CGD), the body (CGB) and the source (CGS) in a trench-gated **DMOSFET** .

Figure 17B is a graph illustrating the gate voltage V9 as a function of gate charge Qg.

Figure 18 is a perspective view of a SSA trench **DMOSFET** in a stripe geometry with a "ladder" P+ source-body design and a thick bottom...

...polysilicon diode arrangements for voltage-clamping the gate to the source of a trench-gated **MOSFET** . Figure 20C shows a cross-sectional view of a polysilicon diode arrangement.

Figure 21 A illustrates a cross-sectional view of SSA trench **DMOSFET** with a thick oxide 0 layer at the bottom of the trench overlapping a heavily...

...Figure 22 is a diagram of a process flow for manufacturing an SSA

trench **DMOSFET** , including variants.

Figure 23 is a cross-sectional view of an SSA trench **DMOSFET** , including an active cell array, a gate bus, a polysilicon ESD diode and an edge...

...illustrate cross-sectional views of a step-by step process for manufacturing an SSA trench **DMOSFET** , including an active cell array, a gate bus, a polysilicon ESD diode and an edge...

...thick oxide layer on the bottom.

Figure 26A shows the dopant profile in a conventional **MOSFET** .

Figure 26B shows the dopant profile in a **MOSFET** formed using a chained body implant in accordance with an aspect of this invention.

Figures 27A-27D **MOSFET** structures that can be fabricated using a high pressure 1 0 process for depositing a metal contact layer.

Figures 28A-28D illustrate the steps of a process of fabricating another **MOSFET** in accordance with the invention.
Description of the Invention
1 5 Figures I OA and...

...where a new technique is required to form the contact feature in the active trench **DMOS** transistor cells. If this were possible, the limit of such a construction would be set...

...0 um capable wafer fab is needed to manufacture a 32 Mcell/in 2 trench **DMOS** , while a 0 urn fab is needed for 180 Mcell/in2 designs. In this context, the term "O.6 @Lrn fab" refers to the feature size of the highest density **CMOS** IC process that the a facility is capable of producing, with the requisite level of problems of manufacturing reliable, high yield, ultra dense power **MOSFETs** .

Figures 1 1 A- I I E illustrate the basic elements of a process of forming a super-selfaligned (SSA) trench **DMOSFET** . The process describes a method to form a dense array of trench capacitors with access...

...the silicon mesa regions.

This SSA capacitor is consistent with the formation of trench-gated **DMOSFETs** but is not limited as such. For example, the SSA array could be used in insulated gate bipolar transistors (IGBTs), **MOS** -gated bipolar devices, and other types of devices.

A nitride layer 102 (or a layer...

...limited.

-14 As will be understood, Figures I I A- I I E show several **MOSFET** cells of an array which would typically include millions of cells in a power **MOSFET** . As shown, the structure produced is a large area capacitor which is a structural element of a trench power **MOSFET** .

The trench is then oxidized to form a sacrificial oxide (not shown) to reduce any...

...junctions.

Such details will be described below for the exemplary fabrication of a trench power **MOSFET** . Next, the exposed surface of the polysilicon gate II 2 is oxidized to form a...mask. This is evident from a comparison of Figure 12A, which shows a conventional trench **DMOSFET** , and Figure 1213, which shows a mesa according to this invention with a metal layer...
...oxide is "below" the silicon surface. 5 A known figure of merit for a power **MOSFET** is the area-to-width ratio A/W, which is a measure of the

area...

...die required to provide a given "channel width" (roughly speaking, the total perimeter of the **MOSFET** cells). A comparison of various device designs can be performed using the A/W ratio as an indicator of the device performance and **on - resistance** .

The smaller the A/W, the better the performance. 0 Figure 13 makes this A ...

...densities approaching 1 billion cells per square inch (1Gcells/in") are anticipated as realistic trench **DMOS** structures for manufacturing, using the invention described herein. Applying these methods. the scaling of such...

...photolithographic technology.

Figures 15A- 1 5D illustrate cross-sectional views of a variety of trench **DMOS** designs,.each with a uniform gate oxide thickness along the trench sidewalls and bottom. In...16A illustrates the phenomenon of field plate induced (FPI) breakdown in thin gate oxide trench **DMOS** devices. As shown in Figure 16A, ionization in FPI limited devices occurs at the trench...

...to hot carrier damage and oxide wearout.

Another disadvantage of a thin gate oxide trench **DMOSFET** is the resulting overlap capacitance between the gate and the drain, and the increase in...

...is needed to do so.

An embodiment of this invention is shown in Figure 18. **MOSFET** 180 is formed in a 5 stripe design in an N-epitaxial layer 188. with...source design of Figure 19C reduces the N+ contact and the channel perimeter further, compromising **on - resistance** to achieve enhanced ruggedness. The minimum manufacturable mesa width for this design is preferably around...

...the geometries and device features discussed thus far, a preferred embodiment of an SSA trench **DMOSFET** is expected to exhibit structural and electrical characteristics as summarized in.the Table 1.
Table5o A to 7oo A) High transconductance
oxide Low channel resistance
Low threshold
No **punchthrough**
ESD protection Poly diode Protects thin gates
ESD tolerance
DC overvoltage clamp
The ESD protection...

...a polysilicon layer and electrically shunting the gate to source electrodes of the trench power **DMOS** . Below a specified voltage, typically 6 to 8-V per series-diode pair, the diodes...

...the N+ from the source implant as the N+ cathode, and likely using a dedicated **P** -type **implant** as the anode doping to set the value of the breakdown. The diodes D5-D8...

...paralleledforward biased diodes, instead (see Figure 20D).

Figure 2 1 A illustrates an SSA trench **DMOSFET** 2 1 0 with the N buried layer NBL 212 0 overlapping the thick oxide layer 214 at the bottom of the gate trench to achieve an improved **on - resistance** in lower breakdown voltage devices (especially for avalanche breakdown voltages below 12 V), by eliminating...

..but before the deposition of the second polysilicon layer.

-22 Fabrication of an SSA trench **DMOSFET** is outlined in the flow chart of Figure 22.

Included are major blocks associated with...

...are thus not meant to be limiting.

A cross-sectional view of an SSA trench **MOSFET** produced by this process sequence is shown in Figure 23. While the device shown is an N-channel SSA trench **DMOS** , the flow 2 0 can also produce an SSA P-channel device by substituting N...polysilicon layer 278 that is in the diode region 280 is moderately doped with a **P** ,, anode **implant** and selectively counterdoped by the N+ source implant to form a 0 series of diodes...

...electrode 272 via strapping metal layer 273. Since the gate and source of a power **MOSFET** are typically shorted together when the device is biased in the off condition, the operation...Range Target Requirement P-channel
Nitride layer 274 500 to 3ooo A 2000A 13' body **implant** **P** + body
deposition must penetrate implant must
(CVD) (thickness) Good oxide etch penetrate
selectivity
Oxide layer...MeV range phosphorus
1013 to 1014 1013 CM-2
Body implant cm- 6* After difftision; **P** ' **implant** ;
(conventional) 2; 60 to 150 **keV** 80 **keV** **400** to 900 K2/sq. 120 keV
B+
Body implant (high 8 X 1012 to 8...

...body charge for a given threshold voltage, thereby reducing the vulnerability of the device to **punchthrough** breakdown. This technique also has the advantage that the depth of the source-body junction...

...to a first order, affect the threshold voltage of the device, as it does in **DMOS** devices formed with conventional diffused body processes. The body-drain junction can be targeted at the same depth as in a conventional diffused-body **MOSFET** . The maximum implant energy is -2 9chosen to penetrate the nitride and set the junction...deposition of pOlysilicon layer 278. The polysilicon layer 278 is doped with a blanket anode **implant** of **P** -type impurity (not shown), so that polysilicon layer becomes P-type except where layer 278...same
5) contact openings in 2 @Lrn features on gate
nitride layer 276 contact bus
P + (13) **implant** 20 to 80 keV BF2+ Xj < 0.8 xj (P+)< xj (N+) As+
(energy and...

...poly
P+ Body Contact Formation
This is an optional process step (not shown) wherein the **P** + **implant** regions are 2 0 selected by a mask rather than going into every contact (as...

...Target Requirement P-channel
P+ mask Blocks BF2 2 @trn Defines body Blocks As
(photoresist) **Implant** feature contact **implant**
P + **implant** (energy 20 to 80 keV BF2+ 0. 8 No depth As+
and dose) 7*10...

...in conjunction the SSA techniques described herein, in Region I.

Fig. 27A illustrates a trench **MOSFET** wherein a contact with a mesa has a submicron width, even though the oxide layer...of the invention. In Figure 28A. after the SSA process has been completed, the trench **MOSFET** has been coated with a glass layer 420, which could for example be borophosphosilicate glass...

Claim

I A process for fabricating a trench **MOSFET** comprising:
providing a body of semiconductor material having a surface;
forming a first mask over...

...and the remaining portion of the polysilicon layer.

19 A process for fabricating a trench **MOSFET** comprising:
providing a semiconductor body having a surface;
1 0 forming a first mask over...

...with an upper surface of the first oxide layer. -3 9
. A trench-gated power **MOSFET** comprising;
a semiconductor body having a trench formed therein, a wall of the trench intersecting...and the top surface extending laterally to the trench comer.

23 The trench-gated power **MOSFET** of Claim 22 wherein a lower surface of the 0 second portion of the gate...

...below a level of the surface of the semiconductor body.
24 The trench-gated power **MOSFET** of Claim 23 wherein an upper surface of the second portion of the gate oxide...

...the level of the surface of the semiconductor S body.

25 The trench-gated power **MOSFET** of Claim 22 wherein the gate oxide layer
comprises a third portion
adjacent a bottom...

...the third portion being thicker than the first portion.
0

26 The trench-gated power **MOSFET** of Claim 25 wherein an upper surface of the third portion is at a level...

...the junction between the body region and the drain region.

27 A trench-gated power **MOSFET** comprising;
5 a semiconductor body having a major surface and a trench forined in the
...
...in contact with the top surface of the semiconductor body.

28 The trench-gated power **MOSFET** of Claim 27 wherein a lower surface of the second portion of the gate oxide...

...level of the surface of the semiconductor 1 5 body.

29 The trench-gated power **MOSFET** of Claim 28 wherein an upper surface of the second portion of the gate oxide...

...above the level of the surface of the semiconductor body.

30 The trench-gated power **MOSFET** of Claim 27 wherein the gate oxide layer
comprises a third portion
adjacent a bottom...

...third portion being thicker than the first portion. 2 5 31. The trench-gated power **MOSFET** of Claim 30 wherein an upper surface of the third portion is at a level...

...the junction between the body region and the drain region.
32 A trench-gated power **MOSFET** comprising;
a semiconductor body having a major surface and a trench formed in the

3...

...trench, the second portion being thicker than the first portion.

33 The trench-gated power **MOSFET** of Claim 32 wherein an upper surface of the second portion is at a level...

...junction between the body region and the drain region.

34 A method of fabricating a **MOSFET** comprising:
providing a semiconductor body;
0 forming a trench in a surface of the semiconductor...

...barrier layer on a surface of the mesa.
0

37 A method of fabricating a **MOSFET** comprising:
providing a semiconductor body;
forming a trench in a surface of the semiconductor body...practicable, search terms used)
USPTO APS, EAST, NPL
seach terms: power mcisfet, buried gate power **mosfet** , self aligned power **mosfet** , etc.
C. DOCUMENTS CONSIDERED TO BE RELEVANT
Category* Citation of document, with indication, where appropriate...
?

?t s25/ti,pn,pd,an,ad,au,pa,ae,k/3

25/TI,PN,PD,AN,AD,AU,PA,AE,K/3 (Item 3 from file: 348)

Power MOSFET **and fabrication method**
Leistungs- MOSFET **und Herstellungsverfahren**
MOSFET **de puissance et methode de fabrication**

PATENT ASSIGNEE:
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PATENT (CC, No, Kind, Date): EP 890994 A2 990113 (Basic)
EP 890994 A3 000202
APPLICATION (CC, No, Date): EP 98203152 911219;
PRIORITY (CC, No, Date): US 631573 901221; US 631569 901221

ABSTRACT EP 890994 A2
A submicron channel length is achieved in cells having sharp corners, such as square cells, by blunting the comers of the cells. In this way, the three dimensional diffusion effect is minimized, and **punch through** is avoided. Techniques are discussed for minimizing defects in the shallow junctions used for forming hte short channel, including the use of a thin dry oxide rather than a thicker steam thermal over the body contact area, a field shaping p+ diffusion to enhance breakdown voltage, and TCA gettering. Gate-source leakage is reduced with extrinsic gettering on the poly backside, and intrinsic gettering due to the choice of starting material.

Power MOSFET **and fabrication method**
Leistungs- MOSFET **und Herstellungsverfahren**
MOSFET **de puissance et methode de fabrication**

...ABSTRACT comers of the cells. In this way, the three dimensional diffusion effect is minimized, and **punch through** is avoided. Techniques are discussed for minimizing defects in the shallow junctions used for forming...

...SPECIFICATION to the fabrication of such circuits, with particular reference to the fabrication of low defect **DMOSFET** structures.
Power **MOSFET** devices enjoy widespread use in such applications as automobile electrical systems, power supplies, and power...

...220AB case. The technology used to fabricate the SMP60N05 product is characterized by a specific **on - resistance** of 3.5 micro-ohms/cm2.
Many different processes have been used for the fabrication of power **MOSFET** devices over the years. These are generally deep diffusion processes. For example, in one early...

...1980 and naming Lidow et al. as coinventors, a p+ tub region is about 4 **microns** deep and a p+ body region is about 3 **microns** deep. The cell configuration is hexagonal.
The technology used to fabricate the SMP60N05 product typically achieves junction depths range from 2.5 to 5 **microns** for the body, from 5 to 6 **microns** for the p+ body contact, and from 0.5 to 1 **micron** for the n+ source regions. The cell configuration is square.
The present invention facilitates the realization of a reduced rDS(on))) and a higher **MOSFET** cell density, which promotes more efficient load management switching and allows the use of smaller...
...the present invention facilitates the realization of a lower gate charge for the same specified **on - resistance** of earlier devices, which allows the use of small drive circuits and fewer components.
These...

...embodiment, a method for initially oxidizing a silicon body with steam for forming a power **MOS** device, gettering is performed with 1 - 6 percent TCA at 1000 - 1250 degrees C. In another embodiment directed to forming thin gate oxide of a power **MOS** device, gettering is performed with 0.5 - 5 percent TCA at a temperature in the...

...degrees C. In another embodiment directed to forming a p- body diffusion in a power **MOS** device, gettering is performed with 0.5 - 5 percent TCA at a temperature in the...

...degrees C. In another embodiment, a heavily doped p+ region of less than 2.5 **micron** junction depth is formed for a power **MOS** device with the steps of boron injection, boron soak, and low temperature oxidation in the...

...is greater than 120 degrees. In another embodiment, a method for forming a silicon power **MOS** device on a silicon body, comprises the steps of forming a first mask overlaying the...

...and in which:

Figure 1 is a schematic representation of a general n-channel power **MOSFET** with its simplified resistive equivalent circuit;

Figure 2 is a graph showing three voltage ratios...

...present invention;

Figure 18 is a cross-sectional view of the periphery of a power **MOSFET** device in accordance with the present invention; and

Figures 19-20 are plan views of a completed power **MOSFET** device, in accordance with the present invention.

A cross-sectional structure of an n-channel power **MOSFET** with its simplified resistive equivalent circuit is illustrated in Figure 1. A n-type lightly...

...18 is provided over the drain and portions of the body, the latter functioning as **MOSFET** channel regions. The principal elements of the simplified resistive circuit include the channel resistances 20...

...23 and 24, and the epi resistance 26.

Figure 2 is a graph showing the **on - resistance** contribution of the channel regions 20 and 21, the JFET region 22, 23 and 24, and the epi region 26 for an arbitrary 60 volt n-channel **DMOSFET** . Vos)) is 10 volts, temperature is 25 degrees C, each square cell measures 10 **microns** by 10 **microns** , and the cell space is 6 **microns** . Curve 30 represents ...curve 34 represents the ratio of the epi resistance 26 to RDS)). As is apparent, **on - resistance** is dominated by the channel resistance 20 and 21, the JFET resistance 24 is generally...

...results in reduced channel resistance 20 and 21 and reduced JFET resistance 24 while avoiding **punch - through** due to three dimensional effects at the cell corners. A typical square cell such as...

...square cells of any given device is in the range of from about 1.5 **microns** to about 4 **microns** , reflecting the comparatively deep drivein used to form the variously doped epitaxial regions described above...

...p-type diffusion which is strongly driven in to a depth of from 2.5 **microns** to 5 **microns** . Generally, p-type dopant diffuses horizontally at a rate of about 80 percent of vertical...

...diffusion to a comparatively shallow depth on the order of from 0.5 to 1 **micron** . Moreover, n-type material tends to diffuse to about the same extent horizontally as vertically...

...44 to be made generally short, the three dimensional diffusion effect likely would result in **punch - through** at the corners. **Punch - through** is a condition in which the depletion region reaches into the n+ source,

thereby causing conductance through the reverse-biased device and leading to device breakdown. **Punch - through** would occur because the three dimensional diffusion effect would cause the channel 44 to be...

...three dimensional effect is rendered less problematic at the critical corners, the diffusions are kept **shallow** and the length of **channel** 144 brought into the range of from 0.5 to 0.75 **microns** , for example. Typical junction depths in this event would be about 2.5 - 3 **microns** for the p-tub 160, about 2 - 2.5 **microns** for the p+ body contact 158, about 1 - 1.25 **microns** for the p body 150, and about 0.3 - 0.6 **microns** for the n+ source region 152. Note that normally a heavily doped shallow region such...such as, for example, a dry oxide etch. The resist is suitably stripped, and the **p** - tub **implant** is 5 made (Figure 9) with Boron at a dose in the range of 1E13...

...Figure 11).
A polysilicon film is deposited to a thickness of 0.3 -0.7 **microns** using any suitable equipment. A polysilicon film also is deposited on the backside, and is...

...of LPCVD nitride 222 followed by a BPSG deposition of about 0.8 - 1.3 **microns** and a BPSG reflow 224 at about 850 - 1000 degrees C (Figure 16). The fifth...This minimizes the contact resistance variation.
These techniques have been used to achieve a specific **on - resistance** of 1.65 milliohms-cm2 for 60 volt devices, and 0.85 milliohms-cm2 for...

CLAIMS 1. A power **MOSFET** comprising:
a monocrystalline semiconductor body having an active area and a peripheral termination area;
a...

...source electrode contacting the active area through openings in the insulating layer.
2. A power **MOSFET** as in Claim 1 wherein the peripheral polycrystalline portion substantially laterally surrounds the gate polycrystalline portion.
3. A power **MOSFET** as in Claim 1 or 2 wherein the active area includes source regions contacting the...

...324) through at least part of the openings in the insulating layer.
4. A power **MOSFET** as in any of Claims 1-3 wherein the **MOSFET** contains a group of cells, each comprising:
a gate structure comprising part of the gate...

...junction with the particular source region along its lateral and lower periphery.
5. A power **MOSFET** as in Claim 4 wherein the device region in each cell comprises:
an annular first...

...into the semiconductor body to a greater depth than the first portion.
6. A power **MOSFET** as in any of Claims 1-5 wherein the semiconductor body comprises silicon.
7. A...third mask window consisting substantially of part of the second mask window.
20. A power **MOSFET** comprising:
a semiconductor body having an active area and a peripheral termination area;
a first...

...above the termination area; and
a drain electrode contacting the semiconductor body.
21. A power **MOSFET** as in Claim 20, wherein the termination area includes an inactive region that forms a...

...electrode through the opening in the insulating layers above the termination area.

22. A power **MOSFET** as in Claim 21, wherein the inactive region comprises a field ring that substantially laterally...

...the active area above the outer lateral edge of the field ring.

23. A power **MOSFET** as in Claim 20, 21 or 22, wherein (a) the second polycrystalline portion substantially laterally...

...portion substantially laterally surrounds the second polycrystalline portion.

24. A termination structure for a power **MOSFET**, the termination structure comprising:

a first insulating layer overlying a semiconductor body of a first...

...first insulating layer to a contact region of the polysilicon field ring.

25. A power **MOSFET** comprising:

a monocrystalline semiconductor body having an active area and a peripheral termination area;

a...

...source electrode contacting the active area through openings in the insulating layer.

26. A power **MOSFET** as in Claim 25, wherein the peripheral polycrystalline portion substantially laterally surrounds the gate polycrystalline portion.

27. A power **MOSFET** as in Claim 26, wherein the active area includes source regions contacting the source electrode through at least part of the openings in the insulating layer.

28. A power **MOSFET** as in Claim 25, 26 or 27, wherein the **MOSFET** contains a group of cells, each comprising:

a gate structure comprising part of the gate...

...junction with the particular source region along its lateral and lower periphery.

29. A power **MOSFET** as in Claim 25, 26 or 27, wherein the device region in each cell comprises:

...

?

```
?ds

Set     Items   Description
S1          1   AU='HERMAN THOMAS E'
S2        119   AU='HERMAN T'
S3          3   AU='HERMAN, THOMAS BRUCE':AU='HERMAN, THOMAS STEPHEN'
S4         82   AU='HERMAN, T.'
S5        205   S1:S4
S6          1   S5 AND (MOSFET OR MOS)
?show files
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
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         (c) 2002 ProQuest Info&Learning
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File  77:Conference Papers Index 1973-2002/Sep
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         (c) 2002 The HW Wilson Co.
File 108:AEROSPACE DATABASE 1962-2002/Aug
         (c) 2002 AIAA
File 144:Pascal 1973-2002/Sep W3
         (c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Aug
         (c) 2002 Cambridge Scient. Abstr
File 305:Analytical Abstracts 1980-2002/Aug W4
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Jul
         (c) 2002 DECHEMA
?t s6/9/1
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6/9/1 (Item 1 from file: 8)
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00932137 E.I. Monthly No: EI8007056551 E.I. Yearly No: EI80090126
Title: POWER MOSFET **TECHNOLOGY.**
Author: Lidow, A.; **Herman, T.** ; Collins, H. W.
Corporate Source: Int Rectifier Corp, El Segundo, Calif
Source: Int Electron Devices Meet, 25th, Tech Dig, Washington, DC, Dec 3-5 1979 Publ by IEEE (Cat n 79CH1504-OED), New York, NY, 1979 p 79-83
Publication Year: 1979
Language: ENGLISH
Journal Announcement: 8007

Abstract: The recent development of high performance power **MOSFET** 's threatens the bipolar transistor monopoly on power control. Analysis of the presently available devices reveals several areas of superior performance. Properly designed power **MOSFET** 's exhibit ultra-high speed operation, freedom from second breakdown, excellent temper stability and large avalanche current capability. Near term improvements now under development suggest that power **MOSFET** 's will have a dominant position in the 500 Volt and under power control market. 6 refs.

Descriptors: *TRANSISTORS, FIELD EFFECT; SEMICONDUCTOR DEVICES, MIS
Classification Codes:
714 (Electronic Components)
71 (ELECTRONICS & COMMUNICATIONS)
?

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?ds

Set     Items   Description
S1          1   AU='HERMAN THOMAS E'
S2        119   AU='HERMAN T'
S3          3   AU='HERMAN, THOMAS BRUCE':AU='HERMAN, THOMAS STEPHEN'
S4         82   AU='HERMAN, T.'
S5        205   S1:S4
S6          1   S5 AND (MOSFET OR MOS)
S7          7   AU='DAVIS HAROLD A':AU='DAVIS HAROLD W'
S8        603   AU='DAVIS H'
S9         27   AU='DAVIS, HAROLD':AU='DAVIS, HAROLD (ED. )'
S10       374   AU='DAVIS, H':AU='DAVIS, H.'
S11      1011   S7:S10
S12         8   S11 AND (MOSFET OR MOS)
S13         7   RD (unique items)
S14        39   AU='SPRING K'
S15        64   AU='SPRING, K.':AU='SPRING, K.R.'
S16         3   AU='SPRING, K. S.':AU='SPRING, K.D.'
S17       103   S14:S15
S18         3   S17 AND (MOSFET OR MOS)
S19         3   RD (unique items)
S20         1   AU='CAO JIANJUN'
S21       697   AU='CAO J'
S22         2   AU='CAO, JIANJUN'
S23       724   AU='CAO, J':AU='CAO, J.'
S24      1424   S20:S23
S25         5   S24 AND (MOSFET OR MOS)
S26         5   RD (unique items)
?show files
File   2:INSPEC 1969-2002/Sep W3
         (c) 2002 Institution of Electrical Engineers
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         (c) 2002 NTIS, Intl Cpyrght All Rights Res
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2002/Aug
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File  77:Conference Papers Index 1973-2002/Sep
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File  94:JICST-EPlus 1985-2002/Jul W3
         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/Aug
         (c) 2002 The HW Wilson Co.
File 108:AEROSPACE DATABASE 1962-2002/Aug
         (c) 2002 AIAA
File 144:Pascal 1973-2002/Sep W3
         (c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Aug
         (c) 2002 Cambridge Scient. Abstr
File 305:Analytical Abstracts 1980-2002/Aug W4
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2002/Jul
         (c) 2002 DECHEMA
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13/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6950680 INSPEC Abstract Number: B2001-07-8520B-009
Title: New power MOSFET **technology with extreme ruggeddness and ultra low R/sub DS(on)/ qualified to Q101 for automotive applications**
Author(s): Murray, A.; **Davis, H.** ; Cao, J.; Spring, K.; McDonald, T.
Author Affiliation: Int. Rectifier, HexFET America Fac., Temecula, CA, USA
Conference Title: PCIM 2000. Europe Official Proceedings of the Forty-First International Power Conversion. Conference p.103-7
Publisher: ZM Commun. GMBH, Nurnberg, Germany
Publication Date: 2000 Country of Publication: Germany xiv+610 pp.
ISBN: 3 928643 24 X Material Identity Number: XX-2001-00804
Conference Title: PCIM 2000. Europe Official Proceedings of the Forty-First International Power Conversion. Conference
Conference Date: 6-8 June 2000 Conference Location: Nurnberg, Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P)
Abstract: An extremely rugged technology has been developed for ultra low R/sub DS(on)/ applications. This paper compares the R.A product and ruggedness of this new technology with a previous generation technology. A factor of 2 improvement in R.A product and a factor of 5 improvement in avalanche energy have been demonstrated. The paper also presents a scheme to reliably rate devices under repetitive avalanche conditions. (3 Refs)
Subfile: B
Descriptors: automotive electronics; avalanche breakdown; power **MOSFET** ; semiconductor device reliability
Identifiers: power **MOSFET** technology; ruggeddness; ultra low R/sub DS(on)/; Q101; automotive applications; specific on resistance; repetitive avalanche conditions; avalanche energy; R.A product; device rating
Class Codes: B8520B (Automobile electronics); B0170N (Reliability); B2560R (Insulated gate field effect transistors); B2560P (Power semiconductor devices)
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13/9/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02905702 E.I. Monthly No: EIM9005-021963
Title: High performance BiCMOS circuit technology for VLSI gate arrays.
Author: Gallia, J.; Yee, A.; Chau, K.; Wang, I.; **Davis, H.** ; Moore, K.; Chae, B.; Lemonds, C.; Eklund, R.; Havemann, R.; Bonifield, T.; Graham, J.; Pozadzides, J.; Shah, A.
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Conference Title: Symposium on VLSI Circuits 1989
Conference Location: Kyoto, Japan Conference Date: 19890525
E.I. Conference No.: 13029
Source: Symp VLSI Circuit 1989. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89TH0262-6), Piscataway, NJ, USA. p 9-10
Publication Year: 1989
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 9005
Abstract: The authors discuss the design and technology for a high-density, full BiCMOS channelless gate array. A truly BiCMOS experimental 106K channelless (sea-of-gates) gate array has been developed in 0.8- mu m technology with triple-level metal and local interconnect. A compact gate size of 750 mu m**2 has been used to achieve a core size of less than 0.82 cm**2 with bipolar drivers in every base cell. A gate delay of 360 ps for a 0.4-pF load has been achieved on a 106K-gate (two-input NAND equivalent) test chip. 5 Refs.
Descriptors: LOGIC CIRCUITS--*Design; INTEGRATED CIRCUITS--Fabrication; SEMICONDUCTOR DEVICES, **MOS**
Identifiers: BICMOS CIRCUITS; METAL INTERCONNECTS; DIGEST OF PAPER; GATE

ARRAYS
  Classification Codes:
  721 (Computer Circuits & Logic Elements); 713 (Electronic Circuits);
714 (Electronic Components)
  72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

13/9/5   (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

03554219   INSIDE CONFERENCE ITEM ID: CN037437270
Extremely Rugged MOSFET **Technology with Ultra Low R SUB D SUB S SUB (SUB o SUB n SUB) Specified for a Broad Range of E SUB A SUB R Conditions**
  Murray, A.; McDonald, T.; **Davis, H.** ; Cao, J.; Spring, K.
  CONFERENCE: Power electronics-International conference; 42nd
  PCIM POWER ELECTRONICS CONFERENCE, 2000; 42ND P: 105-114
  Adams/Intertec International, 2000
  ISBN: 0931033780
  LANGUAGE: English DOCUMENT TYPE: Conference Papers
    CONFERENCE LOCATION: Boston, MA 2000; Oct (200010) (200010)

  BRITISH LIBRARY ITEM LOCATION: 6413.612750
  NOTE:
    Presented at Powersystems world 2000 conference & exhibit. Also known as PCIM 2000
  DESCRIPTORS: power electronics; PCIM

13/9/6   (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

03451319   INSIDE CONFERENCE ITEM ID: CN036408273
NEW POWER MOSFET **TECHNOLOGY WITH EXTREME RUGGEDDNESS AND ULTRA LOW R SUB D SUB S SUB (SUB O SUB N SUB) QUALIFIED TO Q101 FOR AUTOMOTIVE APPLICATIONS**
  Murray, A.; **Davis, H.** ; Cao, J.; Spring, K.; McDonald, T.
  CONFERENCE: International power conversion conference; PCIM 2000-41st
  OFFICIAL PROCEEDINGS OF THE INTERNATIONAL POWER CONVERSION -EUROPE -, 2000; 41ST P: 103-108
  ZM Communications GmbH, 2000
  ISBN: 392864324X
  LANGUAGE: English DOCUMENT TYPE: Conference Papers
    CONFERENCE LOCATION: Nurnberg, Germany
    CONFERENCE DATE: Jun 2000

  BRITISH LIBRARY ITEM LOCATION: 6242.257200
  DESCRIPTORS: PCIM; power conversion
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19/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6950680 INSPEC Abstract Number: B2001-07-8520B-009
Title: New power MOSFET **technology with extreme ruggeddness and ultra low R/sub DS(on)/ qualified to Q101 for automotive applications**
Author(s): Murray, A.; Davis, H.; Cao, J.; **Spring, K.** ; McDonald, T.
Author Affiliation: Int. Rectifier, HexFET America Fac., Temecula, CA, USA
Conference Title: PCIM 2000. Europe Official Proceedings of the Forty-First International Power Conversion. Conference p.103-7
Publisher: ZM Commun. GMBH, Nurnberg, Germany
Publication Date: 2000 Country of Publication: Germany xiv+610 pp.
ISBN: 3 928643 24 X Material Identity Number: XX-2001-00804
Conference Title: PCIM 2000. Europe Official Proceedings of the Forty-First International Power Conversion. Conference
Conference Date: 6-8 June 2000 Conference Location: Nurnberg, Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P)
Abstract: An extremely rugged technology has been developed for ultra low R/sub DS(on)/ applications. This paper compares the R.A product and ruggedness of this new technology with a previous generation technology. A factor of 2 improvement in R.A product and a factor of 5 improvement in avalanche energy have been demonstrated. The paper also presents a scheme to reliably rate devices under repetitive avalanche conditions. (3 Refs)
Subfile: B
Descriptors: automotive electronics; avalanche breakdown; power **MOSFET** ; semiconductor device reliability
Identifiers: power **MOSFET** technology; ruggedness; ultra low R/sub DS(on)/; Q101; automotive applications; specific on resistance; repetitive avalanche conditions; avalanche energy; R.A product; device rating
Class Codes: B8520B (Automobile electronics); B0170N (Reliability); B2560R (Insulated gate field effect transistors); B2560P (Power semiconductor devices)
Copyright 2001, IEE

19/9/2 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

03554219 INSIDE CONFERENCE ITEM ID: CN037437270
Extremely Rugged MOSFET **Technology with Ultra Low R SUB D SUB S SUB (SUB o SUB n SUB) Specified for a Broad Range of E SUB A SUB R Conditions**
Murray, A.; McDonald, T.; Davis, H.; Cao, J.; **Spring, K.**
CONFERENCE: Power electronics-International conference; 42nd
PCIM POWER ELECTRONICS CONFERENCE, 2000; 42ND P: 105-114
Adams/Intertec International, 2000
ISBN: 0931033780
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE LOCATION: Boston, MA 2000; Oct (200010) (200010)

BRITISH LIBRARY ITEM LOCATION: 6413.612750
NOTE:
Presented at Powersystems world 2000 conference & exhibit. Also known as PCIM 2000
DESCRIPTORS: power electronics; PCIM

19/9/3 (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

03451319 INSIDE CONFERENCE ITEM ID: CN036408273
NEW POWER MOSFET **TECHNOLOGY WITH EXTREME RUGGEDDNESS AND ULTRA LOW R SUB D SUB S SUB (SUB O SUB N SUB) QUALIFIED TO Q101 FOR AUTOMOTIVE**

APPLICATIONS

Mürray, A.; Davis, H.; Cao, J.; **Spring, K.** ; McDonald, T.

CONFERENCE: International power conversion conference; PCIM 2000-41st

OFFICIAL PROCEEDINGS OF THE INTERNATIONAL POWER CONVERSION -EUROPE -,

2000; 41ST P: 103-108

ZM Communications GmbH, 2000

ISBN: 392864324X

LANGUAGE: English DOCUMENT TYPE: Conference Papers

CONFERENCE LOCATION: Nurnberg, Germany

CONFERENCE DATE: Jun 2000

BRITISH LIBRARY ITEM LOCATION: 6242.257200

DESCRIPTORS: PCIM; power conversion

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26/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6950680 INSPEC Abstract Number: B2001-07-8520B-009
Title: New power MOSFET **technology with extreme ruggeddness and ultra low R/sub DS(on)/ qualified to Q101 for automotive applications**
Author(s): Murray, A.; Davis, H.; **Cao, J.** ; Spring, K.; McDonald, T.
Author Affiliation: Int. Rectifier, HexFET America Fac., Temecula, CA, USA
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Publisher: ZM Commun. GMBH, Nurnberg, Germany
Publication Date: 2000 Country of Publication: Germany xiv+610 pp.
ISBN: 3 928643 24 X Material Identity Number: XX-2001-00804
Conference Title: PCIM 2000. Europe Official Proceedings of the Forty-First International Power Conversion. Conference
Conference Date: 6-8 June 2000 Conference Location: Nurnberg, Germany
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P)
Abstract: An extremely rugged technology has been developed for ultra low R/sub DS(on)/ applications. This paper compares the R.A product and ruggedness of this new technology with a previous generation technology. A factor of 2 improvement in R.A product and a factor of 5 improvement in avalanche energy have been demonstrated. The paper also presents a scheme to reliably rate devices under repetitive avalanche conditions. (3 Refs)
Subfile: B
Descriptors: automotive electronics; avalanche breakdown; power **MOSFET** ; semiconductor device reliability
Identifiers: power **MOSFET** technology; ruggeddness; ultra low R/sub DS(on)/; Q101; automotive applications; specific on resistance; repetitive avalanche conditions; avalanche energy; R.A product; device rating
Class Codes: B8520B (Automobile electronics); B0170N (Reliability); B2560R (Insulated gate field effect transistors); B2560P (Power semiconductor devices)
Copyright 2001, IEE

26/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4803822 INSPEC Abstract Number: A9423-4280L-008, B9412-4130-008
Title: TM mode optical characteristics of five-layer MOS **optical waveguides**
Author(s): Chunsheng Ma; **Cao, J.**
Author Affiliation: Dept. of Electron. Eng., Jilin Univ. of Technol., Changchun, China
Journal: Optical and Quantum Electronics vol.26, no.8 p.877-84
Publication Date: Aug. 1994 Country of Publication: UK
CODEN: OQELDI ISSN: 0306-8919
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The field distribution and complex eigenvalue equation of the TM mode are solved from the wave equation for a five-layer optical waveguide with finite metal cladding and a dielectric buffer layer. For air-Au-SiO/sub 2/-GaAs-AlGaAs **MOS** waveguides, numerical results for the propagation constant and absorption loss of the TM mode are computed in the complex plane from the eigenvalue equation. The effects of some guided structural parameters on the mode propagation and absorption loss are analysed and discussed. (14 Refs)
Subfile: A B
Descriptors: eigenvalues and eigenfunctions; metal-insulator-semiconductor devices; optical constants; optical films; optical losses; optical waveguide theory; optical waveguides
Identifiers: TM mode optical characteristics; five-layer **MOS** optical waveguides; field distribution; complex eigenvalue equation; TM mode; wave

equation; five-layer optical waveguide; finite metal cladding; dielectric buffer layer; air-Au-SiO/sub 2/-GaAs-AlGaAs **MOS** waveguides; propagation constant; absorption loss; complex plane; eigenvalue equation; guided structural parameters; mode propagation; Au-SiO/sub 2/-GaAs-AlGaAs

Class Codes: A4280L (Optical waveguides and couplers); A7865 (Optical properties of thin films); A7820D (Optical constants and parameters); B4130 (Optical waveguides); B2530F (Metal-insulator-semiconductor structures); B5240D (Waveguide and cavity theory)

Chemical Indexing:

Au-SiO2-GaAs-AlGaAs int - AlGaAs int - GaAs int - SiO2 int - Al int - As int - Au int - Ga int - O2 int - Si int - O int - AlGaAs ss - Al ss - As ss - Ga ss - GaAs bin - SiO2 bin - As bin - Ga bin - O2 bin - Si bin - O bin - Au el (Elements - 1,2,2,3,6)

26/9/3 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03598748 Genuine Article#: PQ292 Number of References: 15

Title: TM MODE OPTICAL CHARACTERISTICS OF 5-LAYER MOS **OPTICAL WAVE-GUIDES**

Author(s): MA CS; **CAO J**

Corporate Source: JILIN UNIV,DEPT ELECTR ENGN,NATL INTEGRATED OPTOELECTR LAB/CHANGCHUN 130023//PEOPLES R CHINA/

Journal: OPTICAL AND QUANTUM ELECTRONICS, 1994, V26, N8 (AUG), P877-884

ISSN: 0306-8919

Language: ENGLISH Document Type: ARTICLE

Geographic Location: PEOPLES REPUBLIC OF CHINA

Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences

Journal Subject Category: OPTICS; ENGINEERING, ELECTRICAL & ELECTRONIC

Abstract: The field distribution and complex eigenvalue equation of the TM mode are solved from the wave equation for a five-layer optical waveguide with finite metal cladding and a dielectric buffer layer. For air-Au-SiO2-GaAs-AlGaAs **MOS** waveguides, numerical results for the propagation constant and absorption loss of the TM mode are computed in the complex plane from the eigenvalue equation. The effects of some guided structural parameters on the mode propagation and absorption loss are analysed and discussed.

Identifiers--KeyWords Plus: GUIDED MODES; BUFFER LAYER; WAVE-GUIDES

Cited References:

BATCHMAN TE, 1972, V8, P848, IEEE J QUANTUM ELECT
CASEY HC, 1978, P43, HETEROSTRUCTURE LA B
DRISCOLL WG, 1978, P7, HDB OPTICS
KAMINOW IP, 1974, V13, P396, APPL OPTICS
MASUDA M, 1977, V16, P2994, APPL OPTICS
POLKY JN, 1974, V64, P274, J OPT SOC AM
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TSAO CYH, 1988, V27, P1316, APPL OPTICS
YAMAMOTO Y, 1975, V11, P729, IEEE J QUANTUM ELECT

26/9/4 (Item 1 from file: 65)

DIALOG(R)File 65:Inside Conferences

03554219 INSIDE CONFERENCE ITEM ID: CN037437270

Extremely Rugged MOSFET **Technology with Ultra Low R SUB D SUB S SUB (SUB o SUB n SUB) Specified for a Broad Range of E SUB A SUB R Conditions**

Murray, A.; McDonald, T.; Davis, H.; **Cao, J.** ; Spring, K.

CONFERENCE: Power electronics-International conference; 42nd

PCIM POWER ELECTRONICS CONFERENCE, 2000; 42ND P: 105-114

Adams/Intertec International, 2000

ISBN: 0931033780
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE LOCATION: Boston, MA 2000; Oct (200010) (200010)

BRITISH LIBRARY ITEM LOCATION: 6413.612750
NOTE:
Presented at Powersystems world 2000 conference & exhibit. Also known as PCIM 2000
DESCRIPTORS: power electronics; PCIM

26/9/5   (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

03451319   INSIDE CONFERENCE ITEM ID: CN036408273
NEW POWER MOSFET **TECHNOLOGY WITH EXTREME RUGGEDDNESS AND ULTRA LOW R SUB D SUB S SUB (SUB O SUB N SUB) QUALIFIED TO Q101 FOR AUTOMOTIVE APPLICATIONS**
Murray, A.; Davis, H.; **Cao, J.** ; Spring, K.; McDonald, T.
CONFERENCE: International power conversion conference; PCIM 2000-41st
OFFICIAL PROCEEDINGS OF THE INTERNATIONAL POWER CONVERSION -EUROPE -, 2000; 41ST P: 103-108
ZM Communications GmbH, 2000
ISBN: 392864324X
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE LOCATION: Nurnberg, Germany
CONFERENCE DATE: Jun 2000

BRITISH LIBRARY ITEM LOCATION: 6242.257200
DESCRIPTORS: PCIM; power conversion
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Set      Items   Description
S1         196   AU='DAVIS H':AU='DAVIS H W'
S2          44   AU='SPRING K':AU='SPRING K W'
S3         204   AU='CAO J'
S4         443   S1:S3
S5           5   S4 AND (MOSFET OR MOS)
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200259
         (c) 2002  Thomson Derwent
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5/7/1
DIALOG(R)File 350:Derwent WPIX

014397446 **Image available**
WPI Acc No: 2002-218149/200228

Contact structure used for e.g. MOSFETs, IGBTs and thyristors has a thin conducting separating layer applied to the exposed surfaces of the side wall spacer elements, and a relatively thick aluminum layer

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **DAVIS H** ; HERMAN T; MAIER M; **SPRING K**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10104274	A1	20010816	DE 1004274	A	20010131	200228	B
JP 2001267569	A	20010928	JP 200128220	A	20010205	200228	

Priority Applications (No Type Date): US 2000497735 A 20000204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10104274	A1		6	H01L-029/78	
JP 2001267569	A		5	H01L-029/78	

Abstract (Basic): DE 10104274 A1

NOVELTY - A contact structure has a thin conducting separating layer (100) applied to the exposed surfaces of the side wall spacer elements (63-67); and a relatively thick aluminum layer (101) which is applied over the total active surface and over the thin conducting separating layer.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the production of the contact structure.

Preferred Features: The thin separating layer is made of TiW and stretches over the same region as the aluminum layer. The TiW layer has a thickness of 0.2 microns and the aluminum layer is ten times the thickness of the TiW layer.

USE - Used for a semiconductor component with a gate control, e.g. MOSFETs, IGBTs and thyristors.

ADVANTAGE - The structure is resistant to large temperature fluctuations.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the contact structure.

Side wall spacer elements (63-67)
Conducting separating layer (100)
Aluminum layer (101)
pp; 6 DwgNo 2/2

Derwent Class: U11
International Patent Class (Main): H01L-029/78
International Patent Class (Additional): H01L-021/28; H01L-021/336; H01L-021/60

5/7/2
DIALOG(R)File 350:Derwent WPIX

012192501 **Image available**
WPI Acc No: 1998-609414/199851

Radiation resistant power MOSFET - has gate oxide film with specific thickness and reverse breakdown voltage

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: MERRILL P; **SPRING K A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5831318	A	19981103	US 96687224	A	19960725	199851	B

Priority Applications (No Type Date): US 96687224 A 19960725
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes

US 5831318   A   9 H01L-021/26

Abstract (Basic): US 5831318 A

The **MOSFET** includes a monocrystalline silicon die, having region extending from its upper surface. A pair of laterally spaced regions are extended from upper surface of die. A source region (50) doped with arsenic impurity atoms, is extended from upper surface of die, into respective channel regions formed by boron implantation for depth less than that of channel regions.

A gate electrode is formed on top of gate oxide film (60). A source electrode is connected to each source region. The gate oxide film has thickness greater than 1250 Angstrom , with reverse breakdown voltage of about 250volts or more.

ADVANTAGE - Increases withstand full reverse voltage in transient fashion.

Dwg.13/13

Derwent Class: U11; U12
International Patent Class (Main): H01L-021/26
International Patent Class (Additional): H01L-029/205

5/7/3
DIALOG(R)File 350:Derwent WPIX

010542663   **Image available**
WPI Acc No: 1996-039617/199604

Process for mfr. of radiation-resistant power MOSFET **- forms gate oxide near end of process to avoid thermal cycling and uses arsenic dopant**

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: MERRILL P; **SPRING K A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5475252	A	19951212	US 871629	A	19870108	199604	B
			US 94288585	A	19940810		

Priority Applications (No Type Date): US 871629 A 19870108; US 94288585 A 19940810
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5475252	A		9	H01L-029/78	Cont of application US 871629
					Cont of patent US 5338693

Abstract (Basic): US 5475252 A

A **MOS** -gated semiconductor device having short-circuit current-limiting ballasting comprises a single crystal Si die having a doped upper surface and many laterally spaced, oppositely doped channel regions (44) and a source for each channel (50) of less depth than the channel. A gate electrode (61) on, and insulated from (60), the channel, can invert the channel on voltage application, a metallic electrode (90) connects to each source, which has a relatively high resistance region in-series with the metal electrode, channel and body path, and the metallic electrode forms a Schottky barrier of increased resistance to the relatively high resistance portions to act as parallel ballasting resistor and limit short-circuit current.

USE - In the mfr. of radiation-resistant power **MOSFET** 's for, e.g. free space uses and in nuclear radiation environments.

ADVANTAGE - The **MOSFET** has a high voltage rating, is not susceptible to gate-to-source threshold voltages changes due to ionising radiation, and the ON resistance is not degraded by high neutron fluxes.

Dwg.13/13

Derwent Class: L03; U12; W06
International Patent Class (Main): H01L-029/78
International Patent Class (Additional): H01L-023/48

5/7/4

DIALOG(R)File 350:Derwent WPIX

009995570 **Image available**
WPI Acc No: 1994-263281/199432

Radiation-resistant power MOSFET **mfr. - using arsenic as n-dopant and forming a gate oxide formed later in the process giving** MOSFET **less susceptible to burn-out**

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: KINZER D M; MERRILL P; **SPRING K A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5338693	A	19940816	US 871629	A	19870108	199432	B

Priority Applications (No Type Date): US 871629 A 19870108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5338693	A		9	H01L-021/265	

Abstract (Basic): US 5338693 A

Mfr. comprises: (a) forming a number of spaced channel regions of first conductivity type (1st C.T) into a surface of a semiconductor wafer region of 2nd C.T by process steps which include driving impurities at high temp. to a first depth beneath the surface; (b) forming respective source regions of 2nd C.T. and selected resistance within each of the channel regions by driving impurities into the wafer to a second depth, less than the first depth with an outer periphery of each of the source regions spaced from an outer periphery of its respective channel regions to define channel regions, (c) forming a gate oxide over selected channel areas, and (d) forming a gate electrode over the gate oxide and a source electrode over the source regions, the selected resistance of the source regions being sufficiently high to act as a ballast resistance to prevent device failure due to parasitic-bipolar-transistor-induced current-hogging in one or more of the source regions.

The gate oxide is pref. formed late in the process and is not subjected to high processing steps. As is used as a slowly diffusing N-dopant in preference to P.

USE/ADVANTAGE - Provides a power **MOSFET** with high resistance to ionising radiation or neutron fluxes. The **MOSFET** is made by a process which reduces its susceptibility to change of gate-to-source threshold voltage and to burnout due to ionising radiation. It is rated at a voltage at which on resistance is not substantially increased by high neutron flux.

Dwg.13/13

Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/265

5/7/5

DIALOG(R)File 350:Derwent WPIX

004716817
WPI Acc No: 1986-220159/198634

CMOS ROM sense amplifier bit line isolation scheme - tops latch line to sense amplifier through logic gates to corresponding even or odd bit select lines

Patent Assignee: SGS-THOMSON MICROEL (SGSA); THOMSON COMPONENTS-MOSTEK CORP (MOSS)
Inventor: **DAVIS H L**
Number of Countries: 007 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 191699	A	19860820	EP 86400268	A	19860207	198634	B
US 4651305	A	19870317	US 85700571	A	19850211	198713	
EP 191699	B	19920129				199205	
DE 3683654	G	19920312				199212	

Priority Applications (No Type Date): US 85700571 A 19850211
Cited Patents: 1.Jnl.Ref; A3...8910; No-SR.Pub; US 3983544; US 3993917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 191699	A	E	13		

Designated States (Regional): AT DE FR GB IT NL

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 191699	B				

Designated States (Regional): AT DE FR GB IT NL

Abstract (Basic): EP 191699 B

The sense amplifier receives information and latches output information in response to a latching signal circuit. A bit line arrangement transmits information to the sense amplifier and a bit line select circuit selects which of the bit lines is to connect with the sense amplifier.

The select circuit includes two quote devices for switching between high and low states with gates controlled by the state of the latching signal. One terminates the on state of the selected one of the bit lines.

ADVANTAGE - Reduces latching operation time by not placing an extra delay in the signal path. Allows bit line to remain near positive supply to reduce precharge power. (13pp Dwg.No.0/3)

Abstract (Equivalent): EP 191699 B

A memory circuit arrangement comprising sense amplifier means (66) for receiving information and effective for latching output information in response to a latching signal (LATCH); first and second bit line means (17',17'') effective for transmitting information to said sense amplifier means (66); first and second bit line select means (65,65) for coupling respectively the first and second bit line means to the sense amplifier characterised in that the first and second bit line select means are operable to select which of said bit line means is to be connected to said sense amplifier means, and in that the first and second bit line select means (65,65) are controlled by respective first and second gate means (99,99) said first gate means being interconnected to receive said latching signal and a bit select signal (CAphi) and said second gate means being connected to receive said latching signal and the complement (CAphi) of the bit select signal, whereby one of the first and second bit line select means is rendered nonconductive when the latching signal (LATCH) changes its logic state to activate the sense amplifier means (66). (8pp)

Abstract (Equivalent): US 4651305 A

A LATCH complement line to the sense amplifier is tapped and combined through logic gates with the corresponding even or odd bit select lines. Thus, when LATCH goes active, the effective odd or even bit select line is disabled, in effect disconnecting and isolating the prior selected bit line from the sense amplifier. This reduces the capacitance on the sense amplifier, speeding its latching operation and it does not place an extra delay in the signal path. Aslo it allows the bit line to remain near the positive supply to reduce percharge power. (6pp)h

Derwent Class: U14
International Patent Class (Additional): G11C-007/00; G11C-017/12
?

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?ds

Set      Items   Description
S1          11   AU='HERMAN T'
S2           5   S1 AND MOSFET
S3           3   S1 AND MOS
S4           1   S3 NOT S2
?show files
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200258
         (c) 2002  Thomson Derwent
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?t s2/9/1-5

2/9/1
DIALOG(R)File 350:Derwent WPIX

014397446 **Image available**
WPI Acc No: 2002-218149/200228
XRPX Acc No: N02-167200

Contact structure used for e.g. MOSFETs, IGBTs and thyristors has a thin conducting separating layer applied to the exposed surfaces of the side wall spacer elements, and a relatively thick aluminum layer

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: DAVIS H; **HERMAN T** ; MAIER M; SPRING K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10104274	A1	20010816	DE 1004274	A	20010131	200228	B
JP 2001267569	A	20010928	JP 200128220	A	20010205	200228	

Priority Applications (No Type Date): US 2000497735 A 20000204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10104274	A1		6	H01L-029/78	
JP 2001267569	A		5	H01L-029/78	

Abstract (Basic): DE 10104274 A1

NOVELTY - A contact structure has a thin conducting separating layer (100) applied to the exposed surfaces of the side wall spacer elements (63-67); and a relatively thick aluminum layer (101) which is applied over the total active surface and over the thin conducting separating layer.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the production of the contact structure.

Preferred Features: The thin separating layer is made of TiW and stretches over the same region as the aluminum layer. The TiW layer has a thickness of 0.2 microns and the aluminum layer is ten times the thickness of the TiW layer.

USE - Used for a semiconductor component with a gate control, e.g. MOSFETs, IGBTs and thyristors.

ADVANTAGE - The structure is resistant to large temperature fluctuations.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the contact structure.

Side wall spacer elements (63-67)
Conducting separating layer (100)
Aluminum layer (101)
pp; 6 DwgNo 2/2

Title Terms: CONTACT; STRUCTURE; **MOSFET** ; THYRISTOR; THIN; CONDUCTING; SEPARATE; LAYER; APPLY; EXPOSE; SURFACE; SIDE; WALL; SPACE; ELEMENT; RELATIVELY; THICK; ALUMINIUM; LAYER
Derwent Class: U11
International Patent Class (Main): H01L-029/78
International Patent Class (Additional): H01L-021/28; H01L-021/336; H01L-021/60
File Segment: EPI
Manual Codes (EPI/S-X): U11-C03A; U11-C09C

2/9/2
DIALOG(R)File 350:Derwent WPIX

013180020 **Image available**
WPI Acc No: 2000-351893/200031
XRAM Acc No: C00-107289
XRPX Acc No: N00-263632

Low voltage MOS gate controlled semiconductor component, useful for a direct voltage/direct voltage converter, employs planar strip technology and has a minimal power index

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **HERMAN T**
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19953620	A1	20000511	DE 1053620	A	19991108	200031	B
JP 2000156383	A	20000606	JP 99318931	A	19991109	200035	
TW 434902	A	20010516	TW 99119463	A	19991108	200170	
US 6346726	B1	20020212	US 98107700	P	19981109	200219	
			US 99436302	A	19991108		

Priority Applications (No Type Date): US 98107700 P 19981109; US 99436302 A 19991108

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19953620	A1		11	H01L-029/78	
JP 2000156383	A		25	H01L-021/336	
TW 434902	A			H01L-029/772	
US 6346726	B1			H01L-029/76	Provisional application US 98107700

Abstract (Basic): DE 19953620 A1

NOVELTY - A MOS gate controlled semiconductor component having gate strips (61) lying over invertible channel region pairs formed by source diffusions (81) in parallel spaced-apart base strip diffusions (80) is new.

DETAILED DESCRIPTION - A semiconductor component with MOS gate control comprises a silicon wafer with an upper first conductivity type layer (52) accommodating boundary layers. Parallel spaced-apart second conductivity type base strip diffusions (80) are formed in the upper surface of the layer (52) and first conductivity type source diffusions (81) are formed in and extend over the same length as the base strip diffusions (80) to form invertible channel regions (82) along the sides of each of the base strip diffusions (80).

Gate strips, comprising gate oxide strips covered by conductive polysilicon strips (61), lie over spaced-apart pairs of adjacent invertible channel regions (82) and the space between their respective base diffusions (80).

INDEPENDENT CLAIMS are also included for the following:

(i) a process for producing the above component; and

(II) a d.c./d.c. converter circuit employing components as described above.

USE - As a low voltage power semiconductor component with MOS gate control, useful for h.f. applications e.g. in a direct voltage/direct voltage converter having a control **MOSFET** and a synchronous rectifier **MOSFET** for producing a regulated d.c. voltage for battery-powered portable electronic equipment such as laptop computers.

ADVANTAGE - The component employs planar strip technology and has a minimal power index (i.e. the product of the gate charge Qg and the switch-on resistance RDSON).

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a semiconductor component according to the invention.

Main wafer body (51)
Upper layer (52)
Gate oxide strip (61)
Base strip diffusion (80)
Source diffusion (81)
Invertible channel region (82)
pp; 11 DwgNo 8/12

Title Terms: LOW; VOLTAGE; MOS; GATE; CONTROL; SEMICONDUCTOR; COMPONENT; USEFUL; DIRECT; VOLTAGE; DIRECT; VOLTAGE; CONVERTER; EMPLOY; PLANE; STRIP ; TECHNOLOGY; MINIMUM; POWER; INDEX
Derwent Class: L03; T01; U11; U12; U13; U24
International Patent Class (Main): H01L-021/336; H01L-029/76; H01L-029/772; H01L-029/78

International Patent Class (Additional): H01L-027/088; H01L-029/94; H01L-031/062; H01L-031/113; H01L-031/119; H02M-003/10
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-H01; L04-E01A
Manual Codes (EPI/S-X): T01-L01; T01-M06A1A; U11-C18A3; U12-D02A; U12-Q; U13-D02; U24-D01A; U24-D02A

2/9/3
DIALOG(R)File 350:Derwent WPIX

004032436
WPI Acc No: 1984-177978/198429
XRPX Acc No: N84-132837
Solid state AC relay - has thyristors controlled by transistors with capacitive potential divider input circuit
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **HERMAN T** ; WILLIAMS O
Number of Countries: 014 Number of Patents: 022
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3345449	A	19840712	DE 3345449	A	19831215	198429	B
FR 2538170	A	19840622				198430	
GB 2133641	A	19840725	GB 8333998	A	19831221	198430	
NL 8304376	A	19840716				198432	
SE 8306952	A	19840723				198432	
BR 8307043	A	19840731				198438	
DK 8305858	A	19840806				198438	
JP 59151463	A	19840829	JP 83241790	A	19831221	198441	
US 4535251	A	19850813	US 82451792	A	19821221	198535	
GB 2133641	B	19861022				198643	
GB 2174242	A	19861029	GB 864263	A	19860220	198644	
GB 2174242	B	19870610				198723	
IL 70462	A	19870916				198747	
CA 1234420	A	19880322				198816	
CH 664861	A	19880331				198816	
CA 1237170	A	19880524				198825	
US 4779126	A	19881018	US 86908867	A	19860912	198844	
DE 3345449	C	19890817	DE 3348348	A	19831215	198933	
DE 3348348	A	19891102	DE 3348347	A	19831215	198945	
DE 3348347	A	19891109				198946	
IT 1194526	B	19880922				199107	
KR 9004197	B	19900618				199127	

Priority Applications (No Type Date): US 83555025 A 19831125; US 82451792 A 19821221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3345449	A		60		

Abstract (Basic): GB 2133641 A
A solid state a.c. relay comprising first and second thyristors each having respective anode and cathode electrodes and a respective gate circuit, characterised in that each of said thyristors is formed in separate respective first and second semiconductor chips and is of the lateral conductivity type, wherein said anode and cathode electrodes of each of said thyristors are on the same first surface of their said first and second chips respectively; said first surface of said first and second chips being optically sensitive, whereby said first and second chips can be switched to conduct current by illuminating said one surface; said solid state relay further comprising a light emitting diode arranged to illuminate said first surfaces upon its energisation; a pair of a.c. terminals; said anode and cathode electrodes of said first and second thyristors connected to said pair of a.c. terminals and in anti-parallel relation with one another; a pair of control terminals insulated from said a.c. terminals

and connected to said light emitting diode; and first and second control circuits connected to said gate circuits of said first and second thyristors respectively for clamping said first and second gate circuits respectively to prevent firing of said first and second thyristors when the voltage between said pair of a.c. terminals exceeds a given value and for clamping said first and second gate circuits in response to transient pulses having a dV/dt greater than a given value.

DE 3345449 A

The solid state relay comprises two separate and identical thyristors connected in antiparallel. The thyristors are optically switched and have anode and cathode electrodes in the same upper surface.

Each of the thyristors is controlled by a **MOSFET** transistor with a capacitive potential divider input circuit. The thyristors will not fire when its surface is illuminated whilst the control transistor is off.

The input to each transistor comprises a capacitor and zener diode connected in parallel. The relay has a lateral structure and is formed on an aluminium oxide substrate. ADVANTAGE - Voltage spikes due to inductive loads are suppressed and optical sensitivity is optimised.

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Abstract (Equivalent): GB 2133641 B

A solid state a.c. relay comprising first and second thyristors each having respective anode and cathode electrodes and a respective gate circuit, characterised in that each of said thyristors is formed in separate respective first and second semiconductor chips and is of the lateral conductivity type, wherein said anode and cathode electrodes of each of said thyristors are on the same first surface of their said first and second chips respectively; said first surface of said first and second chips being optically sensitive, whereby said first and second chips can be switched to conduct current by illuminating said one surface; said solid state relay further comprising a light emitting diode arranged to illuminate said first surfaces upon its energisation; a pair of a.c. terminals; said anode and cathode electrodes of said first and second thyristors connected to said pair of a.c. terminals and in anti-parallel relation with one another; a pair of control terminals insulated from said a.c. terminals and connected to said light emitting diode; and first and second control circuits connected to said gate circuits of said first and second thyristors respectively for clamping said first and second gate circuits respectively to prevent firing of said first and second thyristors when the voltage between said pair of a.c. terminals exceeds a given value and for clamping said first and second gate circuits in response to transient pulses having a dV/dt greater than a given value.

GB 2174242 B

A lateral thyristor which is optically fired, comprising a chip of semiconductor material having a junction-receiving surface of one conductivity type; an anode region of the other conductivity type and a base region of said other conductivity type each formed into said surface with said base region being configured to have at least two opposing sides and said anode region being laterally spaced from said opposing sides of said base region; an emitter region of said one conductivity type formed in and totally contained within said base region and extending therein from said surface; anode and cathode electrodes connected to said anode and emitter regions respectively and radiation means for illuminating at least a portion of said surface for turning on said thyristor; an auxiliary region of said other conductivity type formed in said surface and laterally spaced from and surrounding said base region; and means for resistively connecting said auxiliary region to said cathode electrode.

Abstract (Equivalent): US 4779126 A

The optically triggered lateral thyristor consists of a number of individual lateral thyristor elements connected in parallel. Each element has an active base region which contains a respective cathode region. Each of the base regions is carried in a common conductivity type body. Extending fingers of a continuous anode electrode partly enclose each individual base region to enable the parallel connection

of the individual devices. The thyristor base and emitter zones are surrounded by an auxiliary P region which is resistively connected to a field plate and the cathode electrode to improve emitter collection efficiency.

The cathode electrode and anode electrode are interdigitated. The cathode electrode is connected to spaced, parallel, generally rectangular emitter regions which are disposed in respective bases between loops of the cathode electrode. Radiation applied to the surface of the device by a noncritical photo source produces the effect of a gate current in order to turn on the device.

ADVANTAGE - Injection efficiency of emitter is improved. (13pp)

US 4535251 A

The solid state a.c. relay has two separate and indentical power thryistors connected in anti-parallel arrangement.

The power thyriston are optically switched, lateral conduction devices with anode and cathode electrodes on the same surface. Both are switched by illuminating their surface by reflected illumination from an LED.

Each thyristor is provided with a respective control circuit which includes a **MOSFET** transistor for clamping its respective thyristor gate wherever the voltage across the thryistor exceeds a given absolute value or whenever there is a high dV/dt transient across the thyristor.

The control circuit for the control transistor includes a capacitance divider, one element of which is the distributed capacitance of the control transistor.

The control circuit components can be integrated into the same semiconductor chip which contains the respective power thyristor.

Each of the two identical power chips and the LED chip are spaced from one another and mounted on an alumina substrate.

Two lead wires are stitch-bonded to the electrode pads of the two chips to connect them in anti-parallel relation, and are then stitch-bonded to two respective conductive sections on the alumina substrate.

(9pp

Title Terms: SOLID; STATE; AC; RELAY; THYRISTOR; CONTROL; TRANSISTOR; CAPACITANCE; POTENTIAL; DIVIDE; INPUT; CIRCUIT

Derwent Class: U11; U12; U14; U21

International Patent Class (Additional): H01H-047/00; H01L-027/14; H01L-029/74; H01L-031/10; H03K-017/72

File Segment: EPI

Manual Codes (EPI/S-X): U11-D; U12-A02B; U12-D01B; U14-H03; U21-B01C

2/9/4

DIALOG(R)File 350:Derwent WPIX

003468343

WPI Acc No: 1982-16287E/198209

High current MOSFET **with low forward resistance - has high conductivity channel with uniform lateral doping under gate oxide**

Patent Assignee: INT RECTIFIER CORP (INRC)

Inventor: **HERMAN T** ; LIDOW A

Number of Countries: 009 Number of Patents: 014

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2082385	A	19820303	GB 8124588	A	19810812	198209	B
DE 3131727	A	19820311	DE 3131727	A	19810811	198211	
FR 2488733	A	19820219				198212	
SE 8104485	A	19820322				198214	
JP 57109376	A	19820707				198233	
CA 1165900	A	19840417				198420	
GB 2082385	B	19850206				198506	
US 4593302	A	19860603	US 80178689	A	19800818	198625	
CH 656745	A	19860715				198634	
US 4680853	A	19870721	US 86869109	A	19860530	198731	

DE 3131727	C	19871112				198745
IT 1139374	B	19860924				198823
SE 457035	B	19881121				198849
US 4593302	B1	19980203	US 80178689	A	19800818	199812

Priority Applications (No Type Date): US 80178689 A 19800818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2082385	A		22		
US 4593302	B1		2	H01L-029/76	

Abstract (Basic): GB 2082385 A
A high current **MOSFET** having low forward resistance comprises (a) a semiconductor chip having parallel surfaces; (b) a lightly doped first-type portion extending from a first surface through (part of) the chip thickness; (c) local second-type regions (220,221) in the first surface, spaced from each other by a symmetric mesh of body portions; (d) first type source regions (170,171) in and of lesser depth than the local regions, with the outer periphery of each a fixed distance from the periphery of the local region to define short conduction channels capable of inversion; (e) a mesh-shaped gate insulator (131) over the mesh between local regions and overlapping the short channels; (f) a mesh-shaped gate electrode (132) on the gate insulator; and (g) a vertical conductive first-type region (130) of higher dopant concn. than the body, extending from under the gate insulator between adjacent local regions to a depth less than the local regions, and having constant dopant concn. laterally across the first surface below the insulating layer.

Constant lateral doping concn. provides reduced parasitic base resistance without variation of gate width, increasing avalanche energy and reducing second breakdown problems, for high power switching.

22

Title Terms: HIGH; CURRENT; **MOSFET** ; LOW; FORWARD; RESISTANCE; HIGH; CONDUCTING; CHANNEL; UNIFORM; LATERAL; DOPE; GATE; OXIDE
Index Terms/Additional Words: METAL; OXIDE; SEMICONDUCTOR; FIELD; EFFECT; TRANSISTOR
Derwent Class: L03; U12
International Patent Class (Main): H01L-029/76
International Patent Class (Additional): H01L-021/42; H01L-029/36
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D03A; L03-D03D; L03-D04A
Manual Codes (EPI/S-X): U12-D02A

2/9/5
DIALOG(R)File 350:Derwent WPIX

002332951
WPI Acc No: 1980-D9392C/198018
Power MOS FET system structure - uses high blocking voltage and has low switching resistance attained by common region of relatively higher conductivity (NL 15.4.80)
Patent Assignee: INT RECTIFIER CORP (INRC); LIDOW A (LIDO-I); HERMAN T (HERM-I)
Inventor: **HERMAN T** ; LIDOW A; RUMENNIK V
Number of Countries: 016 Number of Patents: 046
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 2940699	A	19800424				198018	B
NL 7907472	A	19800415				198018	
GB 2033658	A	19800521				198021	
DK 7903506	A	19800512				198023	
SE 7908479	A	19800519				198023	
BR 7906338	A	19800624				198028	
FR 2438917	A	19800613				198030	
IL 58128	A	19811231				198211	

CA 1123119	A	19820504				198221	
CA 1136291	A	19821123				198251	
GB 2033658	B	19830302				198309	
US 4376286	A	19830308	US 78951310	A	19781013	198312	
			US 81232713	A	19810209		
CS 7906589	A	19821029				198313	
HU 24978	T	19830428				198322	
CH 642485	A	19840413				198420	
NL 175358	B	19840516				198423	
DE 2954481	A	19850926				198540	
SE 8503615	A	19850726				198550	
DE 2940699	C	19860403				198615	
US 4642666	A	19870210				198708	
CH 660649	A	19870515				198725	
US 4705759	A	19871110				198747	
JP 63023365	A	19880130				198810	
DK 8805123	A	19880915				198909	
DK 8805124	A	19880915				198909	
US 4959699	A	19900925	US 89371678	A	19890622	199041	
DE 2954481	C	19901206				199049	
IT 1193238	B	19880615				199104	
US 5008725	A	19910416				199118	
SE 465444	B	19910909				199139	
SU 1621817	A	19910115				199150	
US 5130767	A	19920714	US 7938662	A	19790514	199231	
			US 81243544	A	19810313		
			US 88291423	A	19881223		
			US 91653017	A	19910208		
US 5008725	B	19930112	US 7938662	A	19790514	199305	
			US 81243544	A	19810313		
			US 88291423	A	19881223		
US 5191396	A	19930302	US 78951310	A	19781013	199311	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870828		
			US 89303818	A	19890130		
US 4376286	B	19930720	US 78951310	A	19781013	199330	
			US 81232713	A	19810209		
US 4959699	B	19931012	US 89371678	A	19890622	199342	N
US 5338961	A	19940816	US 78951310	A	19781013	199432	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870828		
			US 89303818	A	19890130		
			US 9317511	A	19930212		
US 4705759	B1	19950214	US 78951310	A	19781013	199512	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
JP 7169950	A	19950704	JP 87106158	A	19791008	199535	
			JP 94246144	A	19791008		
US 5191396	B1	19951226	US 78951310	A	19781013	199606	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870828		
			US 89303818	A	19890130		
US 5598018	A	19970128	US 78951310	A	19781013	199710	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870828		
			US 89303818	A	19890130		
			US 9317511	A	19930212		
			US 94288685	A	19940811		
			US 95470494	A	19950606		
US 5742087	A	19980421	US 78951310	A	19781013	199823	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870828		

			US 89303818	A	19890130		
			US 9317511	A	19930212		
			US 94288685	A	19940811		
			US 95548782	A	19951026		
US 4642666	B1	19981027	US 81232713	A	19810209	199850	N
			US 83471818	A	19830303		
US 4959699	B2	19990119	US 78951310	A	19781013	199911	
			US 81232713	A	19810209		
			US 83456813	A	19830110		
			US 8790664	A	19870827		
			US 89371678	A	19890622		
US 5008725	C2	20010501	US 7938662	A	19790501	200138	
			US 81243544	A	19810313		
			US 88291423	A	19881223		
US 5130767	C1	20010814	US 7938662	A	19790514	200150	
			US 81243544	A	19810313		
			US 88291423	A	19881223		
			US 91653017	A	19910208		

Priority Applications (No Type Date): US 7938662 A 19790501; US 78951310 A 19781013; US 81232713 A 19810209; US 89371678 A 19890622; US 81243544 A 19810313; US 88291423 A 19881223; US 91653017 A 19910208; US 83456813 A 19830110; US 8790664 A 19870828; US 89303818 A 19890130; US 9317511 A 19930212; US 94288685 A 19940811; US 95470494 A 19950606; US 95548782 A 19951026; US 83471818 A 19830303

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4376286	A		11		Cont of application US 78951310
US 5130767	A		8	H01L-029/78	Cont of application US 7938662
					Cont of application US 81243544
					Cont of application US 88291423
					Cont of patent US 5008725
US 5008725	B		3	H01L-029/10	Cont of application US 7938662
					Cont of application US 81243544
US 5191396	A		11	H01L-029/78	Cont of application US 78951310
					Div ex application US 81232713
					Div ex application US 83456813
					Div ex application US 8790664
					Div ex patent US 4376286
					Div ex patent US 4705759
US 4376286	B		3	H01L-029/78	Cont of application US 78951310
US 4959699	B		3	H01L-029/10	
US 5338961	A		13	H01L-029/76	Cont of application US 78951310
					Div ex application US 81232713
					Div ex application US 83456813
					Div ex application US 8790664
					Cont of application US 89303818
					Div ex patent US 4376286
					Div ex patent US 4705759
					Cont of patent US 5191396
US 4705759	B1		1	H01L-021/265	Cont of application US 78951310
					Div ex application US 81232713
					Div ex patent US 4376286
JP 7169950	A		10	H01L-029/78	Div ex application JP 87106158
US 5191396	B1		2	H01L-029/78	Cont of application US 78951310
					Div ex application US 81232713
					Div ex application US 83456813
					Div ex application US 8790664
					Div ex patent US 4376286
					Div ex patent US 4705759
US 5598018	A		12	H01L-029/76	Cont of application US 78951310
					Div ex application US 81232713
					Div ex application US 83456813
					Div ex application US 8790664
					Cont of application US 89303818
					Cont of application US 9317511
					Cont of application US 94288685

			Div ex patent US 4376286
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			Cont of patent US 5191396
			Cont of patent US 5338961
US 5742087	A	13 H01L-029/76	Cont of application US 78951310
			Div ex application US 81232713
			Div ex application US 83456813
			Div ex application US 8790664
			Cont of application US 89303818
			Cont of application US 9317511
			Cont of application US 94288685
			Div ex patent US 4376286
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			Cont of patent US 5191396
			Cont of patent US 5338961
US 4642666	B1	H01L-029/76	Div ex application US 81232713
US 4959699	B2	H01L-029/76	Cont of application US 78951310
			Div ex application US 81232713
			Div ex application US 83456813
			Cont of application US 8790664
			Div ex patent US 4376286
US 5008725	C2	H01L-029/76	Cont of application US 7938662
			Cont of application US 81243544
US 5130767	C1	H01L-029/78	Cont of application US 7938662
			Cont of application US 81243544
			Cont of application US 88291423
			Cont of patent US 5008725

Abstract (Basic): DE 2940699 A

The high power **MOSFET** includes a semiconductor wafer having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type. At least two spaced base regions of opposite conductivity are formed in wafer to a first depth. The space between the base regions defines a common conduction region at a given first semiconductor surface location. Two source regions are formed in each pair of the base regions, and are laterally spaced along the first semiconductor surface to define two channel regions, and are connected to respective electrodes. A gate insulation layer is disposed at least on the two channel regions. A drain conductive region is sepd. from the common region by the relatively lightly doped major body portion.

The common region is relatively highly doped, and extends from the given first semiconductor surface location to a depth greater than the depth of the source region. The resistance to current flow at the junctions between the channel regions and the common region and between the common region and the relatively lightly doped major body portion is reduced.

ADVANTAGE - Epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in source-drain path has relatively high conductivity, reducing on-resistance without effecting breakdown voltage. Impurities for defining source regions are applied in single step

Abstract (Equivalent): US 5598018 A

A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in said at least first and second base regions, respectively, at

first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain electrode connected to said first surface and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include relatively shallow depth regions extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

Dwg.8/10

Title Terms: POWER; MOS; FET; SYSTEM; STRUCTURE; HIGH; BLOCK; VOLTAGE; LOW; SWITCH; RESISTANCE; ATTAIN; COMMON; REGION; RELATIVELY; HIGH; CONDUCTING

Derwent Class: U12

International Patent Class (Main): H01L-021/265; H01L-029/10; H01L-029/76; H01L-029/78

International Patent Class (Additional): H01L-021/26; H01L-021/31; H01L-027/02; H01L-027/10; H01L-029/00; H01L-029/68; H01L-029/94; H01L-031/062; H01L-031/113

File Segment: EPI

Manual Codes (EPI/S-X): U12-D02A

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DIALOG(R)File 350:Derwent WPIX

003757167
WPI Acc No: 1983-753378/198335
XRAM Acc No: C83-084351
XRPX Acc No: N83-155381

Semiconductor device has composite double stepped field plate - reducing equipotential field line curvature on reverse bias

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **HERMAN T** ; LIDOW A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4399449	A	19830816				198335	B

Priority Applications (No Type Date): US 80207124 A 19801117
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4399449	A		14		

Abstract (Basic): US 4399449 A

A semiconductor device having a composite field plate comprises (a) a semiconductor body having a flat surface; (b) a pn junction (53) formed in and terminating on the surface; (c) an insulating layer (50) extending over (part of) the junction; (d) a relatively high conductivity poly-Si layer (60) having a first portion galvanically connected to the surface on only one side of the pn junction and a second portion, continuous with the first, stepped up from the surface to overlie the insulator, terminating in an edge; (e) a second insulating layer (65) extending from an edge overlying the first poly-Si portion and over part of the second portion, including the edge; and (f) a contact metal layer (73) overlying the poly-Si and second insulator, extending beyond the poly-Si edge, where poly-Si and metal are in surface-to-surface contact only in areas on one side of the edge of the second insulator.

The poly-Si and metal define a double stepped field plate, extended beyond the volcanic contact region to reduce curvature of electric field equipotential lines within the body during reverse biasing of the pn junction.

The device withstands increased reverse voltage, close to theoretical maximum for device with guard ring. The device is pref. a diode or power **MOS** transistor.

Title Terms: SEMICONDUCTOR; DEVICE; COMPOSITE; DOUBLE; STEP; FIELD; PLATE; REDUCE; EQUIPOTENTIAL; FIELD; LINE; CURVE; REVERSE; BIAS
Derwent Class: L03; U12
International Patent Class (Additional): H01L-029/40
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D04
Manual Codes (EPI/S-X): U12-E02
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4/9/1

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Number of Countries: 001 Number of Patents: 001
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US 4399449	A	19830816				198335	B

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Derwent Class: L03; U12
International Patent Class (Additional): H01L-029/40
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D04
Manual Codes (EPI/S-X): U12-E02
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